Reconfigurable Universal Sensor Interface for Distributed Wireless Sensor Nodes

Anuradha C. Ranasinghe[#1], Lahiru K. Rasnayake[#2], M. Kalyanapala[#3]
[#]*Department of Electronic and Computer Engineering, Sri Lanka Institute of Information Technology*
New Kandy Rd, Malambe, Sri Lanka

[1]anuradha.r@sliit.lk, [2]lahiru.r@sliit.lk, [3]kalyanapala.m@sliit.lk

***Abstract*— Wireless sensor networks of today play a large role in industrial grade field data acquisition systems. The need for vast sensor compatibility will be an evident requirement as wireless sensor networks go mobile and become autonomous. Current technologies make use of multiple signal conditioning circuits which result in bulky power hungry wireless sensor nodes. This paper presents an implementation of a reconfigurable universal transducer interface based on a CMOS multiplexer network supporting a vast diversity of industrial sensors while being compact and energy efficient, which is conducive to wireless sensor networking. The concept, design scheme, prototype implementation with industrial components and the results of integrating this interface into a prototype wireless sensor node are discussed in this paper to illustrate potential applications in mass scale data acquisition based on wireless sensor networks.**

Keywords— **WSN, Universal Interface, Reconfigurable Hardware, Multiplexers**

I. INTRODUCTION

In today's world Wireless sensor networks (WSN) provide creative means to deploy sensors in vast unimagined areas. The development of WSN although motivated by military purposes [1], is employed in a wide range of real world applications including structural health monitoring (SHM), security and surveillance, scientific research, sustainable technologies and medical instrumentation [2]-[4]. The ability to interact with the physical environment in wireless domain provides more robust and versatile platform over traditional environmental monitoring scheme. Currently, for the implementation of a WSN, the two basic approaches involve usage of nodes with single sensor and multiple sensor capability [5]. A single sensor node may be designed integrating sensor element, signal conditioner and Network Application Processor (NCAP) into one sensor node. Single sensor MEMS (Microelectromechanical Sensor) chips and motes are some examples for such a system. If a node per sensor approach is used, many nodes are required in case different parameters of a certain area are to be monitored. Maintaining such a WSN is quite expensive as well as increases the complexity of the network. So the multi sensor node can be used for such situation. The traditional approach to provide multi sensor capability for a WSN node is by employing several signal conditioning stages to the front end of the circuit where every sensor interface is dedicated to a certain sensor type. Each stage may have a dedicated analog to digital converter (ADC) or a separate analog channel from the micro processor unit. The typical design of a multi parameter WSN node is shown in fig. 1

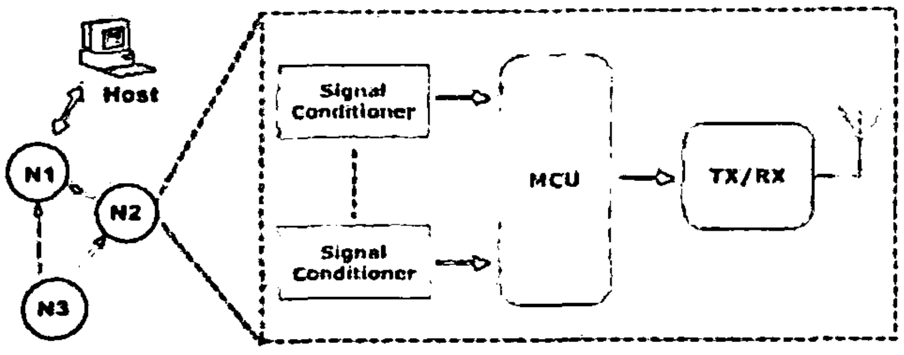

Fig. 1 Typical Design of a Wireless Sensor Node

If the signal conditioner performs a single operation, the functionality of each channel is still limited to a unique data type. If a sensor node cannot provide compatibility to a certain sensor and if the manufacturer does not provide a more capable WSN node to integrate with the current network, this will result in a WSN based on heterogeneous nodes, which is harder to maintain. On the other hand this design scheme is not adequate due to the power consumption, lack of scalability and complexity of the design.

All these design methodologies pose certain difficulties to implement an efficient field data acquisition system. Compared to the traditional hardware design topologies, reconfigurable hardware technologies have shown a certain improvement of designing more flexible devices [6]. Although reconfigurable hardware designs have been adopted in some WSN applications, there is a limited amount of research carried out suggesting reconfigurable hardware designs to solve multi sensing problem. Field programmable gate array (FPGA) based designs are more popular for digital sensors, though they require additional components to facilitate multi sensing operation in mixed signal domain [7]. In the analog domain, two major programmable hardware technologies are the field programmable analog arrays (FPAA) and programmable mixed signal system on chip technology (e.g. PSoC). Both technologies are capable of providing all the common components for supporting different mixed signal processing applications [8]. However these designs cannot be optimized to maintain both accuracy and power consumption. More over signal conditioning, data conversion and data communication may require additional components with both hardware designs which are not very conducive to the Implementation of static or mobile WSNs.

To eliminate these issues we propose a reconfigurable universal transducer interface for wireless sensor nodes which was designed based on ultra low power analog multiplexer network. By using programmable mixed signal hardware architecture, this new approach enables a

978-1-4799-1276-6/13/$31.00 ©2013 IEEE

single channel of this node to obtain signals from a vast diversity of sensors. Currently, the implemented interface has been tested yielding successful results for Thermocouples, Resistive Temperature Device (RTD), Thermistors, Load Cells, Pressure Gauges, Analog Signals, and 4 - 20mA Current Loops. It also ensures homogeneity among WSN nodes. The most significant advantage would be for a node having multiple interfaces because there is no chance for a channel of the WSN node to be left unused since it is reconfigurable which ensures maximum utilization is obtained from a single WSN node. This paper discusses the implementation of this novel approach and the performance of this interface.

II. CONCEPT OF RECONFIGURABLE INTERFACE

In the proposed system, the flexibility of reconfigurable interface is essentially important since it decides the universal functionality and application scope of the data acquisition process of WSN node. The interface circuit was designed to accommodate various types of output signal, provide sensor driving, offset adjustment, data linearization and automatic gain to match the signals and sensitivities of different sensor elements. The trade-off between the measurement accuracy and the flexibility should be optimized so that the resulting system can be widely adaptable to the multi parameter system. Moreover power management of the device is critically important since WSN nodes are deployed in an energy constrained environment [9]. Fig. 2 shows the hardware block diagram of the WSN node where dedicated signal conditioning stages in traditional design were replaced by universal transducer interface module (UTIM).

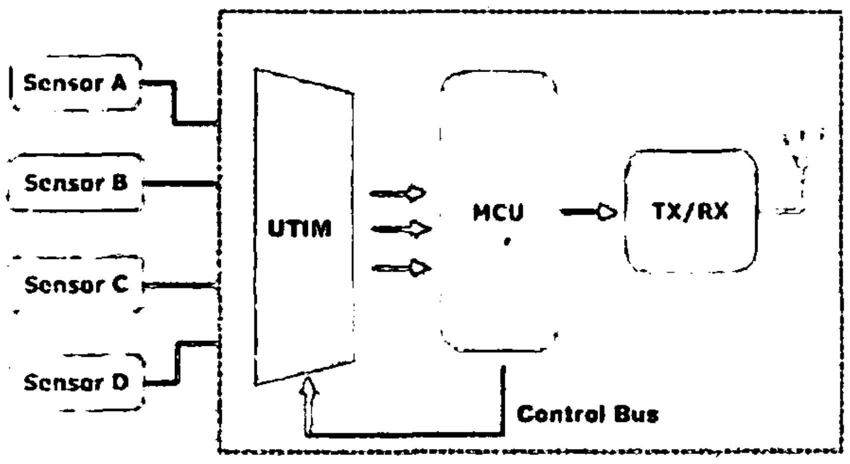

Fig. 2 Proposed WSN Node Design

A. *Mixed Signal Circuit Design*

The UTIM is based on an analog multiplexer network which facilitates the required functionality to perform signal routing between sensor signals and amplifier stages. Time-division-multiplexing will be used to take analog sensor signals from a distributed sensor array periodically so that data can be processed on a common transmission line in a digitally encoded format. These multiplexers were chosen from CMOS logic family because of its high noise immunity and ultra low power profile [10], where the design can be fabricated to be compact with low power, cost effective implementation. Sensor routing is done by writing appropriate logic to the control bus lines of the multiplexers. And also UTIM uses the architecture to synchronize the multiplexing and sampling to ensure a proper settling of the analog data signals while maintaining energy efficiency.

The use of dynamic sensor power cycling with UTIM provides an opening for reducing average power consumption in applications where energy use must be tightly managed and power hungry sensors are interfaced. The average power dissipation, of a transducer is quantified by the following equation:

$$P_{AVG} = DP_{ON} + (1-D)P_{OFF}$$

where D, P_{ON} , and P_{OFF} represent duty cycle, power in normal operation and power in off-mode of the transducer respectively. Selecting appropriate duty cycle by considering settling time of the sensor, the average power of the entire system can be managed to operate in very low level. For instance, considering a load cell (VISHAY Model 9010), P_{AVG} can be greatly minimized while maintaining the measurement accuracy. Table 1 shows the technical data of the load cell.

TABLE I
TECHNICAL DATA OF THE LOAD CELL (VISHAY MODEL 9010)

Parameter	Value
Settling Time	150 mS (Typical)
Operation Power	240 mW
Off-Power	6.8 μW

Taking T_{on} *(Power-on Time) =160mS (settling time + 10mS acquisition time)*, and T_{on+off} *(Cycle time) =1S the* average power can be written:

$$P_{AVG} = (0.16\times 240) + (1-0.16)0.0068mW$$
$$P_{AVG} = 38.405mW$$

The average power consumed by the sensor is approximately 16% of its normal operation power. Hence dynamic power cycling is proven to be energy efficient with the UTIM circuit. Besides that, the arrangement shows in Fig. 3 has number of advantages to eliminate common measurement errors.

- The differential signaling scheme which was used for interfacing signals and amplifiers reduces both environmental noise and multiplexer switching noise.
- Since the on resistance (*Ron*) of multiplexer switches is in series with high impedance input of the amplifiers, *Ron* does not affect to the accuracy of measurement.
- User will be given an option to select preferred excitation supply for sensors. A known fixed current source can be used if the voltage excitation creates considerable voltage drops across *Ron* of the multiplexer switches.
- The sensor is switched to the excitation mode only during the time its measurement taken. That eliminates the self heating errors and continuous power dissipation. However the acquisition time should be greater than sensor settling time.
- When acquiring signals, only one sensor is switched at a time. That prevents creating ground loops among sensors.
- If any sensor requires additional hardware, for better accuracy (e.g. a shunt resistor for linearization and calibration), the four wire channel provides more feasible interface.

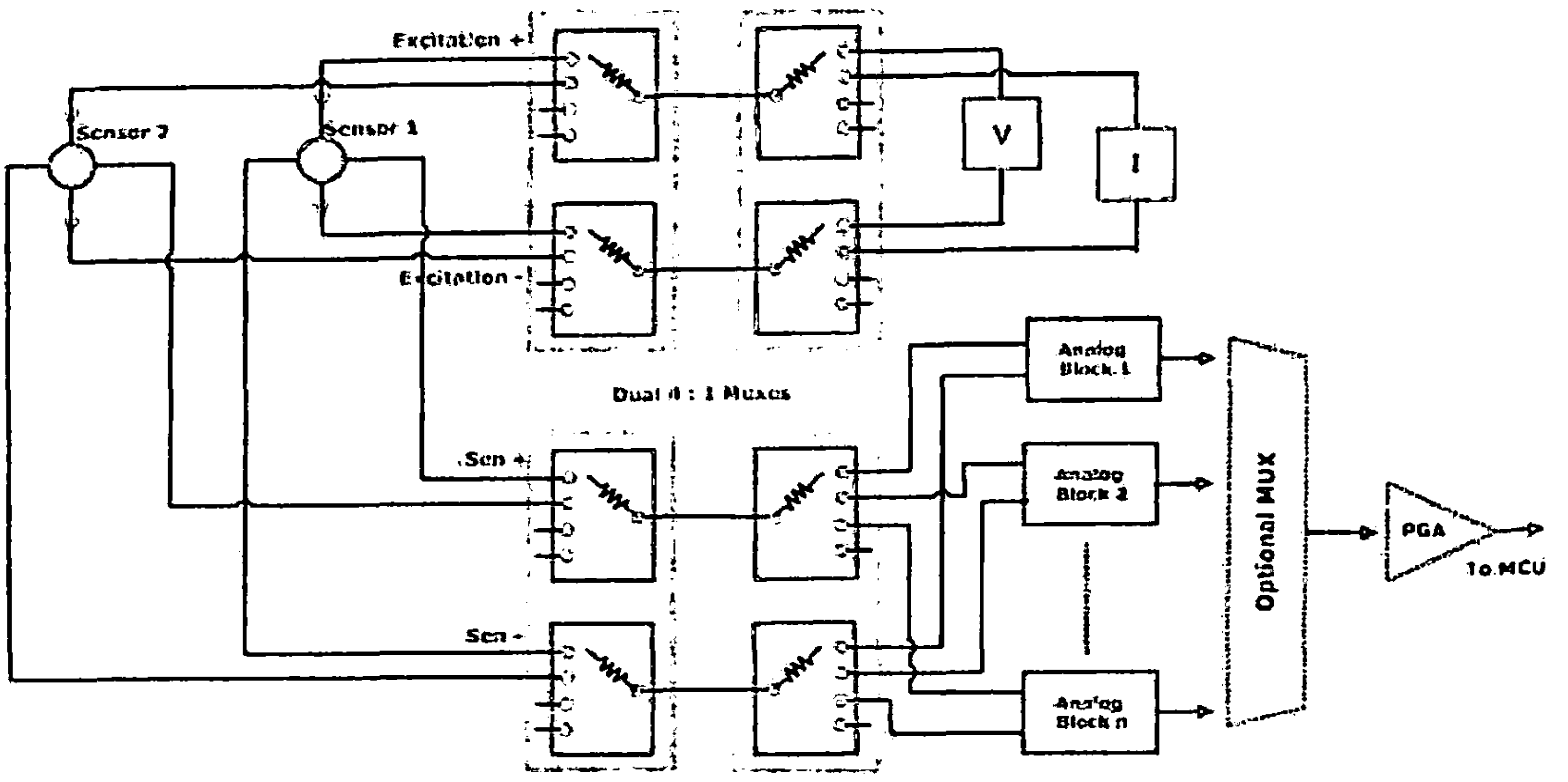

Fig. 3 UTIM Based on Analog Multiplexer Network

The initial design of the UTIM shown in fig. 3 is configured for four analog channels. Each analog channel consists of 4-wire interface, where *Ex+*, *Ex-*, *Sen+*, *Sen-* pins correspond to the terminals of the excitation supply, and the sensor differential signal outputs respectively. These differential signals will be converted into a single ended voltage by routing the signal to an appropriate analog block. Each analog block was design for a specific sensor type which may include Op-Amps, discrete component to provide signal conditioning and filtering before fed into the ADC of the processing unit (MCU). The basic UTIM design may require an optional multiplexer stage, so that only one ADC channel is sufficient to digitize the sensor analog signal.

B. Signal Conditioning Blocks

The multi functioning capability of UTIM is achieved by integrating different signal conditioning blocks at the back end of multiplexer network. Each block converts the sensor signal into a voltage parameter, matches impedances and scales the signal level prior to the ADC input. These analog blocks were designed based on the operational principle and the type of central element of the sensor, so that each block provides more general functions rather than being a dedicated interface type. Besides that, two independent excitation supplies were provided, where selecting is optional. Figure B shows the application of acquiring data from a bridge sensor.

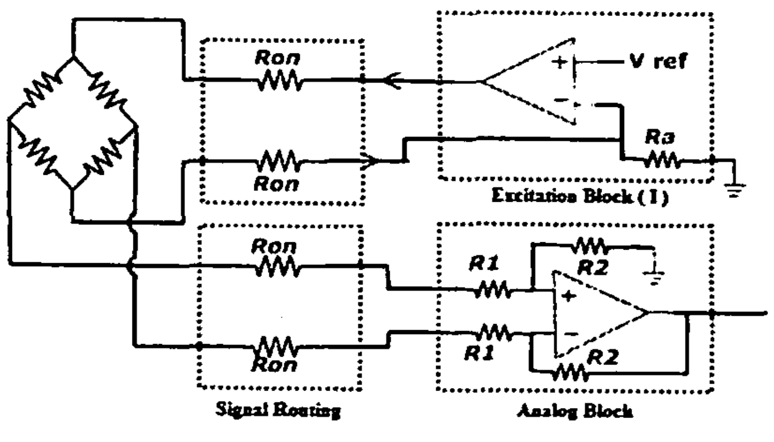

Fig. 4 Bridge Excitation (Constant Current)

Bridge sensor generates quite a weak signal which represents change in resistance of the gauges. If the gauge is powered with voltage excitation, the voltage drops appear in on resistance (Ron) of the multiplexer will cause a significant error to the measurement. In such a situation, it is adequate to drive the bridge with known current excitation where the Ron is not constant. Excitation Block (I) represents a basic current source device made with very few components. For single element varying bridge, the voltage output is given by;

$$V_O = \frac{R_2}{R_1}\left[\frac{V_{REF}}{Ra}\Delta R\right]$$

Programmable Gain Amplifier (PGA) is another important part of a data acquisition system. When dealing with wide range of signal levels, different gain ratios may be required to scale signals for better accuracy [11]. Since most of PGAs available in the market are very expensive, we are proposing a low cost solution based on simple analog components. Following figure shows the design of PGA using a single op amp, analog mux with couple of discrete components.

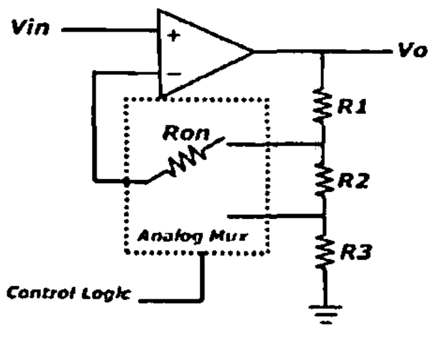

Fig. 5 Low Cost Programmable Gain Amplifier

The control bus line of the multiplexer should be maintained in a logic level to provide the required gain. This design has the advantage of bypassing Ron from the gain stage so that non static Ron will not affect on the measurement. Better performance can be obtained using precision resistors for R1 to R3. This configuration provides two different gain values.

C. Linearization Techniques

Some sensors have the advantage of a very high sensitivity to changes in physical phenomena, and the disadvantage of an aggressively nonlinear characteristic. This might introduce a non linear error to the measurement, which should be eliminated using a proper hardware design or software calibration. Thermistor is a good example for a non linear sensor which has considerable non linearity [12] where the change in the measurement is most rapid at low temperatures, giving great resolution for determining the corresponding temperature values there. At the other end of the range, resistance levels change relatively less with temperature and measurement resolution is relatively poor. Several hardware linearization techniques are available to provide better solution. That will reduce the processing power, memory footprints for lookup tables and polynomial equations [13]. Circuits for linearizing thermistor outputs can be comprised of series, parallel, and series-parallel combinations of fixed resistors and additional thermistors. Following signal conditioning circuit provides a hardware linearization by adding a parallel resistor. Linearization resistor *Rx* value should be equal to the magnitude of the thermistor at the mid-point of the temperature range of interest.

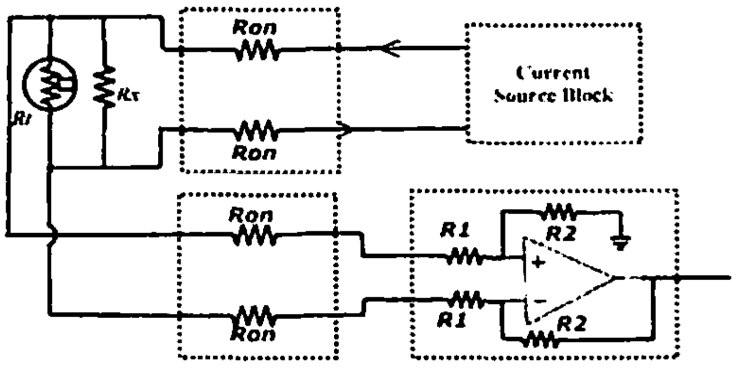

Fig. 6 Thermistor Hardware Linearization

The value of the external resistor can be obtained using following equation;

$$R_X = \frac{[R_{TM}(R_{TL} + R_{TH}) - 2R_{TL}R_{TH}]}{[R_{TL} + R_{TH} - 2R_{TL}R_{TH}]}$$

where R_{TM}, R_{TL} *and* R_{TH} represent thermistor resistances at midpoint, lowest and highest temperature values respectively. Fig. 7 shows the typical response curve of a negative temperature coefficient thermistor and linearization result.

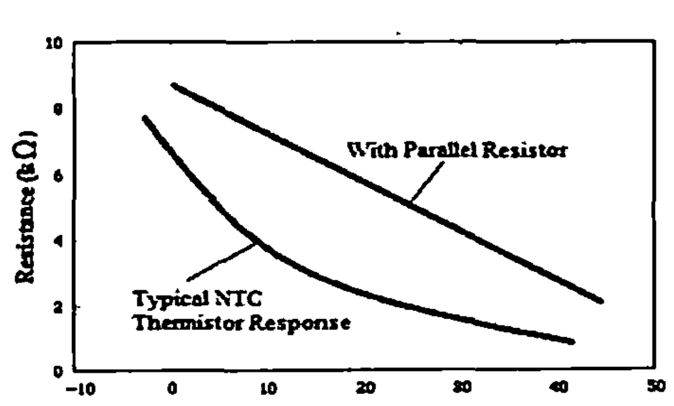

Fig. 7 Linearization Result

Thermocouple is basically two dissimilar metals that are joined together at one end and produce a voltage corresponding to the temperature difference between the open end and the junction end. An additional hardware is required to maintain one junction (normally the cold junction) at a known reference temperature. However this reference temperature is hart to maintain in an embedded mixed signal system environment. Hence proposed device integrates a cold junction compensation interface (AD595) from Analog Device which supports k type thermocouples, provides low impedance, fixed voltage gradient.

III. HARDWARE IMPLEMENTATION AND RESULTS

Since the emphasis of this paper is focused on the benefits of the UTIM, the user may select and integrate other auxiliary peripherals for the WSN node, depending on the application requirements and feasibility. In developing the experimental prototype for this research, the paramount concern was creating a low power design, with universal capability and optimized accuracy. The components used for the UTIM included Dual 4:1 CMOS Analog Multiplexers (MAX4618) for the signal routing stage and a micro power op-amp (LT1079) for optimum power efficiency in this prototype. The performance of this UTIM was tested with the LPC1769 ARM Cortex M3 micro processor from NXP and the XBee ZB module. The LPC1769 has ultra low power profiles for different sleep modes. The power consumption of the UTIM with respect to its switching frequency with different sensor attachments was recorded as shown below in the graph.

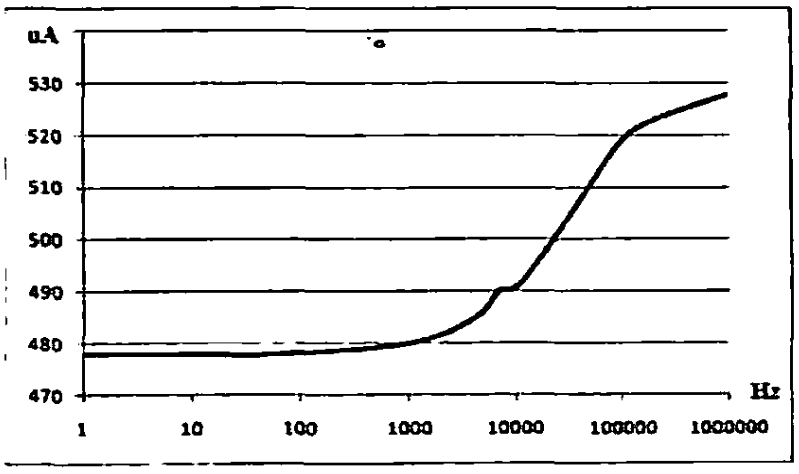

Fig. 8 Power Consumption of UTIM

With the current consumption given in micro amperes (uA) and channel switching frequency in Hertz (Hz) in log-scale, the observations prove that the UTIM is highly power efficient for typical industry grade applications since the current consumption can be maintained as low as 478 uA for adequate switching frequencies. The device performance in high frequencies (10-100MHz) is determined by the frequency responses of individual components. In prototype design, this is limited to 200kHz due to amplifier characteristics. However this frequency limit is more than adequate for low power industry grade applications and this limit is where the optimum performance is preserved. If required, the performance can be extended to higher frequencies by simply replacing the op-amp used.

The prototyped device has been tested with different sensors attached to the universal sensor interface. Test bench included a k type thermocouple (AEM 30-2067), 10k NTC Thermistor (EPCOS B57867S0103 10kΩ @ 25°C), Pt100 RTD (RS 611-8264) and a 20kg Load Cell (VISHAY Model 9010 - 2mV/V). All sensors were tested with both voltage and current excitation supplies. Table 1 shows the measurement accuracy of each sensor with respect to the excitation.

TABLE 2
MEASUREMENT ACCURACY WITH DIFFERENT SENSORS

Sensor	Excitation Type	
	Voltage	Current
K type Thermocouple	No Excitation ±3 C°	No Excitation ±3 C°
Thermistor	±0.7 C° with linearization resistor	±0.4 C° with linearization resistor
Pt100 RTD	±3 C°	±0.4 C°
Load Cell	±250g (≈1.3% full scale)	< 1% full scale

Affect of the *Ron* of multiplexers will reduce the accuracy of low resistive sensors in voltage excitation mode. The accuracy of thermistor measurement can be further improved over a wide temperature range by substituting a thermistor network in place of the single thermistor in the Wheat stone Bridge which provides maximum linear deviation of this circuit is $\underline{+}0.24C^{\circ}$ from 0 C° to 100C°

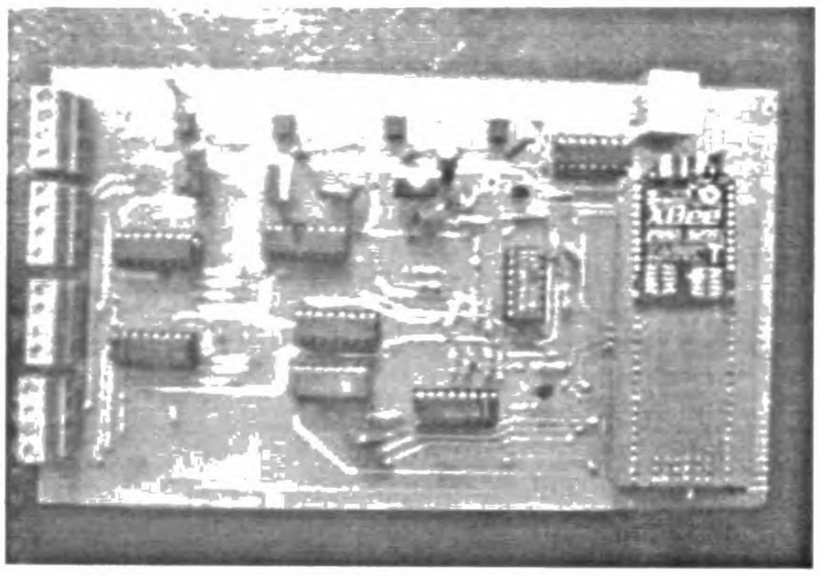

Fig. 9 Prototype Implementation of WSN Node

IV. CONCLUSIONS

The concept of UTIM has proposed a highly flexible front end design for WSN sensor node technology which reconfigures its hardware in an autonomic way to interface with a large range of distributed sensors to solve the multi-sensing challenge in many WSN applications where different types of sensors are to be supported. Power consumption tests prove that UTIM is highly power efficient and can be integrated with an ultra low power processing unit (e.g. Nano Watt) in a WSN node. If the prototype was implemented using surface mount devices, the circuit can be further miniaturized. For future work, the development of adaptive reconfigurable hardware designs, autonomous sensor identification and sensor plug and play technologies will be evaluated to introduce a better deployment for distributed WSN applications.

ACKNOWLEDGMENT

The authors would like to thank the Managing Director of Attotech System Engineering (PVT) Ltd and senior staff of Sri Lanka Institute of Information Technology, Malabe for providing hardware accessories, laboratory facilities to accomplish this task.

REFERENCES

[1] J. T. John and S. R. J. Ramson, "Energy-Aware Duty Cycle Scheduling for Efficient Data Collection in Wireless Sensor Networks", *IJARCET Volume 2, Issue 2, Feb . 2013.*

[2] D. Culler, D. Estrin, and M. Srivastava, "Overview of sensor networks", *IEEE Computer, vol. 37, no. 8, pp. 41–49, 2004.*

[3] N. Xu, S. Rangwala, K. K. Chintalapudi, D. Ganesan, A. Broad,R. Govindan, and D. Estrin, "A wireless sensor network for structural monitoring," *in SenSys '04: Proceedings of the 2nd international conference on Embedded networked sensor systems. ACM Press, 2004,*
pp. 13–24.

[4] D. Malan, T. Fulford-Jones, M. Welsh, and S. Moulton, "Codeblue: Anad hoc sensor network infrastructure for emergency medical care", *inProceedings of the MobiSys 2004 Workshop on Applications of MobileEmbedded Systems (WAMES 2004), June 2004.*

[5] Kay Romer, Friedemann Mattern, "The Design of Wireless Sensor Network", *Institute of Pervasive Computing, IEEE Wireless Communications, Dec. 2004.*

[6] Shenfang Yuan, Lei Qiu, Shang Gao, "Providing Self-Healing Ability for Wireless Sensor Node by Using Reconfigurable Hardware", *MDPI Sensor Journal, Oct.* 2012.

[7] K. M. Iswarya, S. Usha, "Adaptive Runtime Reconfigurable Wireless Sensor Nodes Based On Dynamical Data Aggregation", *IJREAT Volume 1, Issue 1, March. 2013.*

[8] Rentao Wang, Ken Deevy, "Reconfigurable Adaptive Wireless Sensor Node", *ISSC 2012, NUI Maynooth, June 28, 2012*

[9] Yuan Tian, Eylem Ekici, "Energy-Constrained Task Mapping and Schedualling in Wireless Sensor Networks", *IEEE International Conference on Mobile Adhoc and Sensor Systems Conference, Nov. 7 2005.*

[10] Scott Crowder, "Low Power CMOS Process Technology", *IBM, SRDC. East Fishkill, NY*

[11] David A. Sobel, "System and Method for a Programmable Gain Amplifier", U.S. Patent 7026875 B2, Apr 11, 2006.

[12] S. Kaliyugavaradan, P Sankaran, "Hardware linearization of thermistor response using series-parallel resistors for temperature-to-time conversion, *Meas. Sci. Technol.* ***5 (1994) 786-788.*** *Printed in the UK*

[13] Lars E. Bengtsson, "Lookup Table Optimization for Sensor Linearization in Small Embedded Systems", *Journal Sensor Technology, doi:10.4236/jst.2012.24025, Dec.2012.*