FR 1655

Design and Construction of a Signal Meter

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Section 1

Information regarding Project/Project Personnel:

i) Contract Number: RG/2007/SI/02 , TG/SI/002

ii) Title of the Project: Design and Construction of a Signal Meter.

iii) Principal Investigator: Dr. K. D. R. Jagath Kumara

iv) Co-Investigators:

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2. Dr. D. N. Uduwawala

v) Institute(s) where research was being carried out: University of Peradeniya.

vi) Date of award: 01.12.2007

vii) Date of completion of Project: 14.07.2010

viii) Total allocation of funds (Rs): 950,000/=

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x) Number of Research Students employed: 01

xi) Post graduate degree completed with dates: None

xii) Number of Technical Assistants and/or labourers employed and period of service: 09

Section 2:

Executive Summary of the Project

Mobile and wireless communication systems utilize various frequency bands in the UHF region ranging from approximately 0.3 – 3GHz. For example, the 800-900MHz and 1.8GHz bands, which are used by most cellular mobile systems, [1]. In any case, one of the major problems is measuring the received signal strength (RSS) of various sub frequencies. The RSS should be high enough within the cell and the cell edge strength should be according to the specifications. If the cell edge strength is too high, the adjacent channel and co-channel interference degrades the signals in surrounding cells. In addition, excessive RF power may cause health hazards. However, very low power levels may limit the functionality of mobile and wireless equipment.

The aim of this project is to design a wideband RF energy/power meter which can be fabricated mainly in Sri Lanka. The initial prototype constructed for the 300 – 1300MHz (UHF) spectrum, consists of three main modules, a signal acquisition and energy estimation module, a microwave up/down converter and a precision light weight wide band antenna. During the project period, the following modules have been successfully fabricated and tested.

Microwave circuit for up-converting UHF to 2.7GHz with image rejection.

Microwave circuit for down-converting from 2.7GHz to 63MHz

RF circuit for down-converting from 63MHz to 1MHz

2.3GHz micro-strip filter

USB signal reader and Display

5MHz digital clock

Wide band loop antenna

Frequency auto-scanner

1MHz high gain amplifier

5v, 12v and 18v regulated power supplies

The completion of this project ascertains that wideband microwave circuits & antennas and high speed digital circuits can be developed in the DEEE laboratory at the University of Peradeniya.

We acknowledge the financial support received from the National Science Foundation of Sri Lanka under the grant RG/2007/SI/02 over the period from 01.12.2007 to 20.05.2010. A valuable piece of equipment and a considerable range of microwave components, which helped the successful completion of this project, were obtained during the project period.

Contents

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Section 3

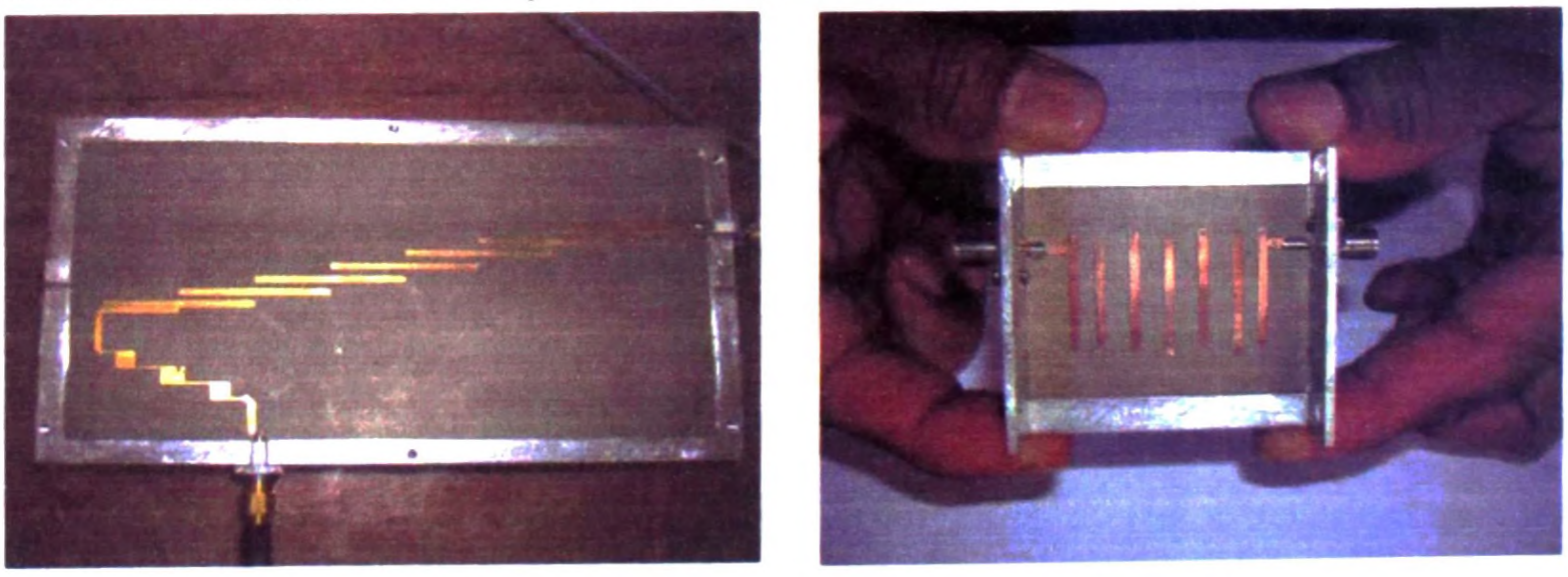
3.i Introduction

When it comes to the electronic industry at radio frequencies (R.F), the technical capability of Sri Lanka was hitherto limited to the lower R.F. frequencies below about 100 MHz. This has serious implications. For equipment such as radar systems, communication equipment, satellite transmitters and receivers, this implies that Sri Lanka has to totally rely on imports. It is true that some of the equipment, especially which are mass-manufactured (eg. hand-held mobile phones, TV receivers etc), there may not be a gain if we try to manufacture them locally. But for high-tech items which are not mass-manufactured, it is a totally different scenario. For example, advanced test equipment like the signal meter developed in this project or radar systems can be locally manufactured at a considerably low cost.

However, Sri Lanka has totally missed in the game of RF design due to several reasons. Firstly, the design at high frequencies, especially in the microwave region (1-30 GHz), requires special techniques, such as considering the wave propagation phenomena in printed circuit board fabrication, scattering parameters for characterizing devices, and measurement techniques which are unique to the microwave region. Until recent times, the necessary theoretical knowledge and the practical skills were not taught anywhere in the Sri Lankan university system. This has resulted in a serious lack of engineers with RF and microwave design capability in Sri Lanka, and we believe this is the primary reason for the lack of any RF or microwave circuit designs.

The second factor contributed adversely to the development of RF and microwave technology is the high cost of the test and measuring equipment, and fabrication and design tools required. However, in the past few years the Department of Electrical and Electronic Engineering (DEEE) of the University of Peradeniya (UP) was addressing these issues and as a result was able to embark on this ambitious project which clearly demonstrates that Sri Lanka can indeed carry out economically viable designs in the challenging field of RF and microwaves. To be specific, the DEEE introduced two courses in microwave circuit design, one at the final year undergraduate level and another at the postgraduate level in 2004, which were the first such coursed introduced in Sri Lanka. The DEEE acquired the essential equipment, namely a microwave vector network analyzer, a photo-plotter, CAD tools from Ansoft, and plated through-hole fabrication equipment utilizing several research grants.

To the best of the author's knowledge, the RF signal energy meter design presented here is the first complete microwave/RF system designed in Sri Lanka. This meter can measure signal energy or power in 300-1300 MHz frequency band. As you will see in the detailed design, some of the circuitry (example, first conversion stage) operates at frequencies as high as 3.6 GHz. As microwave technology is new to Sri Lanka, a large number of subsystems fabricated as part of the project are also the devices fabricated for the first time in Sri Lanka. For example, there are no records of components such as the edge coupled bandpass filter or the inter-digital filter shown below fabricated in Sri Lanka prior to this work.



(a) Edge-coupled filter (b) Inter-digital filter

Figure 3.iv.A0

3.ii Scientific Scope of the Project

The signal meter developed is multi-purpose. It can be used to monitor RF/microwave radiation levels and can also be used as a low-cost spectrum analyzer in a laboratory or a workshop. As the use of wireless equipment (mobile phones, wireless internet, internet TV, satellite TV, wireless phones etc) is growing, it is essential to

ensure that the radiation levels the public is exposed to is within safety limits. This is particularly important as long term exposure to RF/microwave radiation is hazardous [9]. At present, the radiation levels are measured using spectrum analyzers or measuring receivers with calibrated antennas. Although these devices provide accurate measurements, they are expensive. The signal power/energy meter developed in this project is a cost effective alternative.

Apart from the above stated advantages, the work presented extends the technical capability of Sri Lanka. Any RF or microwave system (eg. a radar or a satellite transceiver) comprises the same building blocks, namely, filters, amplifiers, mixers, oscillators, and couplers/combiners. This project demonstrates that we have achieved the technical competency to combine these units to build systems. The successful completion of this sophisticated test equipment suggests that design of other systems such as radar, communication receivers etc are also within the technical capability of Sri Lanka.

3.iii. Relevance to the Objectives and Expected Outputs of Thematic Program

All the components designed and fabricated during the project period are relevant to the thematic program.

Part I

3.iv.A Overall design of the RF front end

We begin the overall design by first stating the design objectives. The design objectives are specified in Table 3.iv.A1.

Design parameter	Targeted value
Frequency range	1-1300 MHz
Dynamic range	70 dB
Final I.F.	1 MHz
Final I.F. bandwidths	500 kHz, 200 kHz, 30 kHz

Table 3.iv.A1: Design Objectives

We designed the RF front end as a super-heterodyne system to exploit the advantages of the super-heterodyne architecture. The first step of the design is selecting the appropriate values for various intermediate frequencies (I.F.), and I.F. filter bandwidths to avoid undesirable interferences such as spurs and harmonics. This is described next.

3.iv.A.1 Selection of frequencies:

3.iv.A.1.1 Selection of frequencies of the 1st stage:

The frequency band we want to measure is from 300 to 1300 MHz (in fact as high as possible). If we try to down convert, the I.F. will fall within the bandwidth we try to measure. For example, suppose we select the I.F. to be 1 GHz. Now, if there is a strong 1 GHz signal present at the input, there will be an unwanted signal at the I.F due to RF to I.F. leakage in the mixer. In addition, frequencies below 1 GHz will have to be up converted while the frequencies between 1-1.3 GHz have to be down converted. We overcome all these problems by selecting an I.F. value outside the range from 0 to 1300 MHz, ie up conversion. There again you have two options.

(a) $f_{IF} = |f_{LO} + f_{RF}|$

(b) $f_{IF} = |f_{LO} - f_{RF}|$

We select case (b) as it has a unique advantage. There won't be any in-band (within IF bandwidth) spurious products due to harmonics of the LO. Of course there can be in-band spurs due to the harmonics of the RF signal. But these are not significant as the RF power level is much less when compared with the LO power level[1]. In fact this is the very reason why the pre-selector of commercial spectrum analyzers is a fixed low-pass filter (rather than tunable) for the low frequency band (see pp44,45, 51 of [3]).

Apart from the above mentioned facts, we need to consider the component options available for mixers and oscillators before finalizing any frequency. An extensive literature review showed that SIM-U742MH is perhaps the best choice we have for the first mixer. Important parameters of SIM-U742 are shown in Table 3.iv.A2.

LO Level (dBm)	Frequency (MHz)			Conversion Loss (dB)			LO-IF Isolation Typ. (dB)		LO-RF Isolation Typ. (dB)		IP3 (dBm)
	(IF) In	LO	(RF) Out	Typ.	σ	Max	Typ	Min.	Typ.	Min	
13	0.1-3300	2300-7400	2300-7400	8.0	0.4	9.8	17	11	23	13	20

Table 3.iv.A2: Specifications of the SIM-U742 mixer from MiniCircuits

[1] Note the LO signal power is +13 dBm while the maximum RF power is -27 dBm (this you will see later).

The mid range of this mixer is from 1-1650 MHz [4]. It can be seen from Table 3.iv.A2, that the IF should be within 2300-7400 MHz. We select 2300 MHz as the I.F. As we select the $|f_{LO} - f_{RF}|$ term, we can obtain the IF by varying LO frequency from 2300-3950 MHz to cover the entire mid-range of the mixer. Note that an LO frequency of 2300 MHz produces the desired IF when the RF is at d.c (ie, not at 1 MHz). Table 3.iv.A3 summarizes the results of a market survey done to find a suitable wideband VCO. Clearly, DCY200400-5 from Synergy is the best choice. However, this particular series of VCOs from synergy is meant to replace Yttrium Iron Garnet (YIG) oscillators used in high end measuring equipment and therefore is expensive. So, as an alternative, we selected ROS-3360 from MiniCircuits in our design. The price we have to pay for the reduced cost is the limitation in the measurement range. The measurement range produced by ROS-3360 is from d.c to 1060 MHz (with LO varied from 2300-3360 MHz). However, we do the system design in such away that it will be valid for both choices. This enables to extend the range simply by replacing the VCO with a DCY200400-5 from Synergy.

Manufacturer	Model	Frequency Range (MHz)	
		Low	High
MiniCircuits	ROS-2800-719	1400	2800
MiniCircuits	ROS-3000-819	2000	3000
MiniCircuits	**ROS-3360**	**2120**	**3360**
Synergy	**DCYS200400-5**	**2000**	**4000**
Synergy	DCY160360-5	1600	3600
Synergy	DCY300600-5	3000	6000

Table 3.iv.A3: Available Oscillators

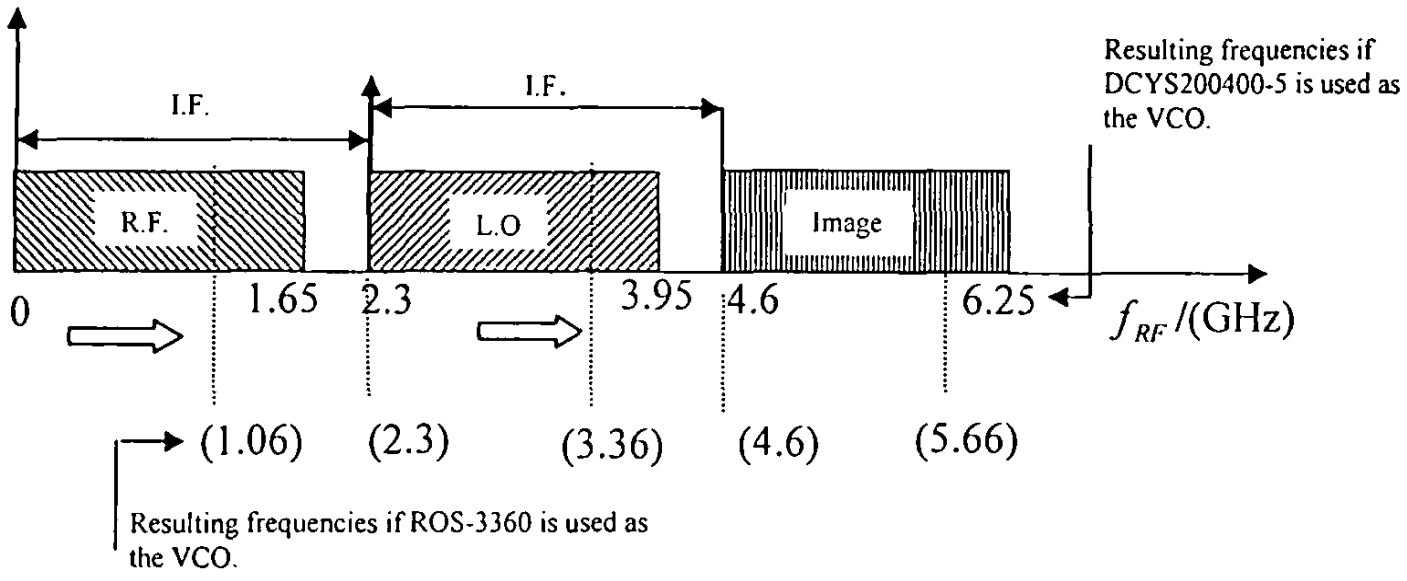


Figure 3.iv.A1: Frequency plan of the first mixer stage

As shown in Figure 3.iv.A1, the I.F. is selected as

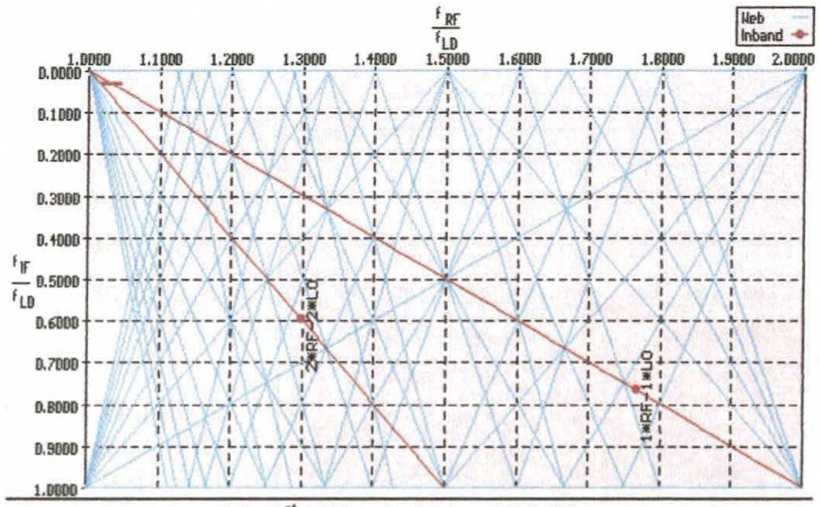
$$f_{IF} = f_{LO} - f_{RF}. \qquad \text{..... Eq. 3.iv.A.(1)}$$

That is, if the input is varied from 0 to 1.65 GHz (or from 0 to 1.06 GHz, if ROS-3360 is used), we keep the I.F. constant at 2.3 GHz by varying the local oscillator frequency from 2.3 GHz to 3.95 GHz (or from or 2.3 to 3.36 GHz). This, we do by using DCYS200400 from Synergy (or ROS-3360 from MiniCircuits) as the VCO.

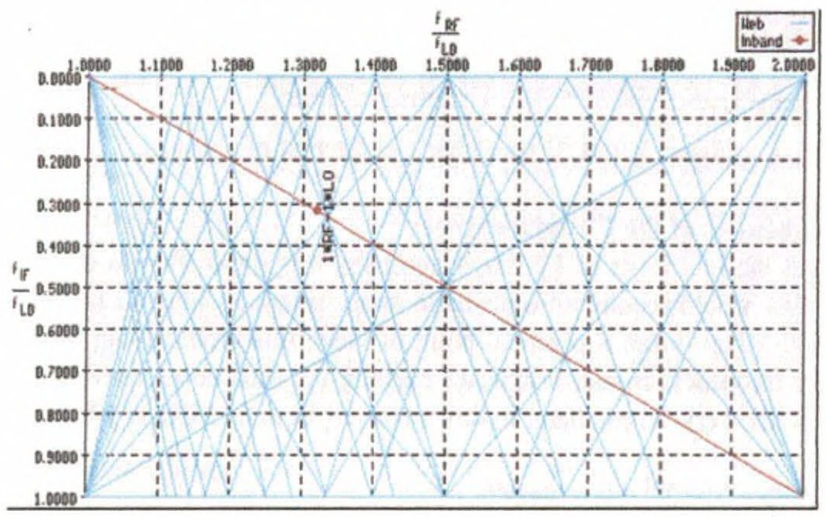
The selection of 2300 MHz as the I.F. has many advantages. The selected I.F. is well separated from the measurement range and therefore there are no leakage signals from RF to IF. Image frequencies are also well separated making image rejection an easy task. As we select the LO and RF difference signal as the IF, there are no in-band spurs due to harmonics of the strong local oscillator signal. Our selection also enables to use LO to IF leakage signal (LO feed through) for calibration purposes [3]. More specifically, LO to IF leakage signal can be used as a maker to show the position of d.c [3]. Finally, the selected IF is 100 MHz away from the ISM (Instrumentation Scientific and Medical) band allocation from 2400-2500 MHz. This minimizes any possible interference from the ISM band.

What should be the first I.F. bandwidth?

To answer this question, we need to look at the second IF stage. First mixer generates a large number of spurious products in addition to the first IF. These can appear as in-band spurs at the second I.F unless they are suppressed prior to entering the second mixer stage.



(a) 1st IF bandwidth = 55 MHz.



(b) 1st IF bandwidth = 40 MHz.

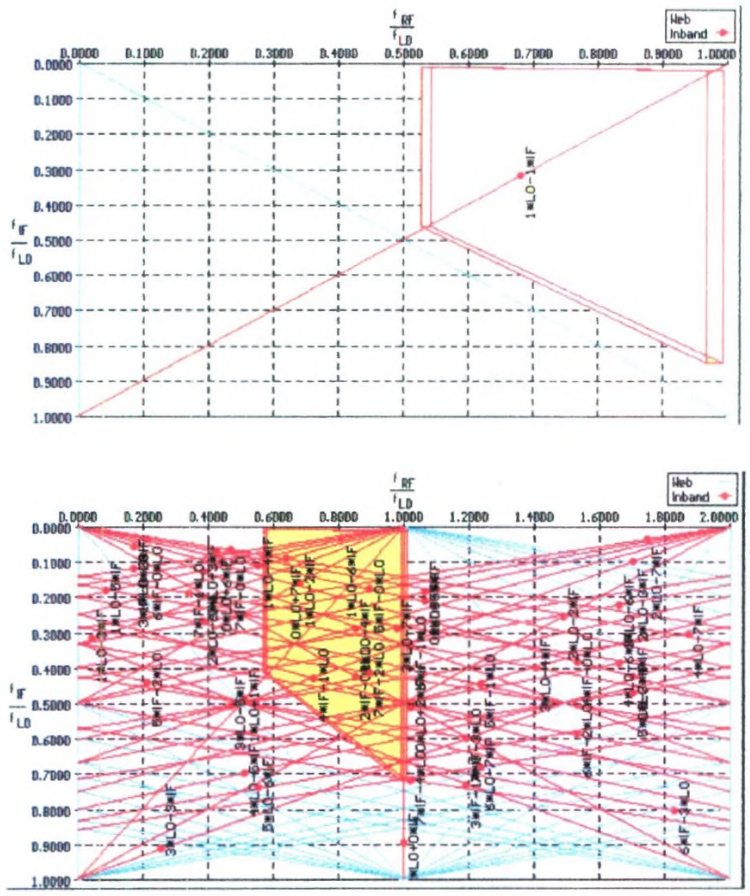
Figure 3.iv.A2: Spur charts of the 2nd mixer stage.

To decide the first IF bandwidth, we use RF Workbench. Second Mixer stage was simulated and the bandwidth of the input filter was adjusted by trail and error to find the maximum bandwidth possible at the input of the second mixer, if in-band spurs are to be avoided. Results are shown in Figure 3.iv.A2. As Figure 3.iv.A2 (a) shows, the first spurious component (it happens to be $2\times RF - 2\times LO$) starts to appear at 55 MHz. So, leaving a margin as well, we selected the first I.F. bandwidth to be 40 MHz. This sets the fractional bandwidth of the first IF filter to 1.74% (40/2300x100).

Spur chart of the first mixer stage

We completed the simulation of the first mixer stage with these values using RF Workbench. The results are shown in Figure 3.iv.A.3. Figure 3.iv.A3 (a) shows the spur chart obtained by considering the local oscillator harmonics up to the 9th order while keeping the harmonic number of the R.F input at 1. The figure clearly shows that there is only one product, the desired I.F. term 1xLO-1xRF, within the trapezium defined by filter bandwidths. However, there is no way you can avoid in-band spurs, if you consider RF harmonics as well. This is shown in Figure 3.iv.A3 (b). Fortunately, we can ignore the effects due to RF harmonics as the level of R.F. harmonics is very low when compared to the L.O. level.

In fact, it is possible to exactly calculate the I.F. levels due to harmonics of the R.F. input, if the spur table of the first mixer is available. Unfortunately, spur table is not available from the manufacturer of the mixer we selected for stage 1 (SIM-U742MH from MiniCircuits). Measurement of the spur table at the DEEE is also not possible at present due to the lack of necessary measuring equipment.



(a) L.O harmonics: 0 to 9

RF harmonics: only 1

(b) L.O. harmonics: 0 to 9

R.F. harmonics: 0 to 7

Figure 3.iv.A.3: Spur charts of the first mixer stage

3.iv.A.1.2 Selection of frequencies of the 2nd mixer stage:

Our final objective is to get the I.F. down to 1 MHz. Obviously, it is impossible to down convert from 2300 MHz to 1 MHz, because that would require an unrealistic image rejection filter (a filter of 2 MHz transition width centered around 2300 MHz). From a practical point of view, this problem can be avoided, if we down convert from a much lower frequency. In our design, we perform the final down conversion to 1 MHz starting from 63 MHz. We use a 64 MHz crystal oscillator to down convert from 63 MHz to 1 MHz in the 3rd stage.

What should be the bandwidth of the 2nd mixer stage?

If we select low-side injection for the second stage, an LO frequency of 2237 MHz is required to down convert from 2300 to 63 MHz. As our final I.F. (ie, the I.F. of the 3rd stage) is 1 MHz, the image frequency of the second stage is at 65 MHz. This means that the second IF filter bandwidth should be narrow enough to suppress any image at 65 MHz while passing the 63 MHz I.F. signal. Although this requires a bandpass filter of fractional bandwidth 3.1 %, this can be accomplished with a surface acoustic wave (SAW) filter. This is exactly what we have done in the design of the 3rd stage.

Spur chart of the second mixer stage

With our selection of the LO and I.F. frequencies (LO=2237 MHz and I.F.=63MHz), input and image frequencies will be at 2300 MHz and 2174 MHz leaving a 106 MHz (2280 – 2174) margin to suppress the image[2]. We selected the second I.F. bandwidth to be 0.4 MHz to match with the bandwidth of a commercially available SAW filter. Figure 3.iv.A.2(b) shows the spur chart corresponding to a second I.F. of 63 MHz and a bandwidth of 0.4 MHz. Our selection here is the best you can imagine with no in-band spurs. Figure 3.iv.A2(b) was obtained considering both RF and LO harmonics up to the 9th order.

3.iv.A.1.3 Selection of frequencies of the 3rd mixer stage:

In the third stage, we down convert from 63 MHz to 1 MHz using a 64 MHz local oscillator. The I.F. bandwidth at 1 MHz is selected to be 200 kHz. The resulting spur chart is shown in Figure 3.iv.A4. The figure shows that only the desired term is present and the 3rd IF is also free from spurs. It is interesting to note the necessity of a SAW filter in the 2second stage. If you used an ordinary LC filter in place of the SAW filter, the factional bandwidth would be around 5%. For a 63 MHz centre frequency, this means a bandwidth of approximately3.1MHz. Figure 3.iv.A5 shows the spur chart of the 3rd stage if the SAW filter is replaced by an ordinary LC filter. The figure clearly illustrates how the signal is corrupted by a large number of in-band spurs.

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[2] Note, we selected 2280 MHz instead of the 2300 MHz (first IF frequency) taking the 40 MHz bandwidth of the first IF filter into account.

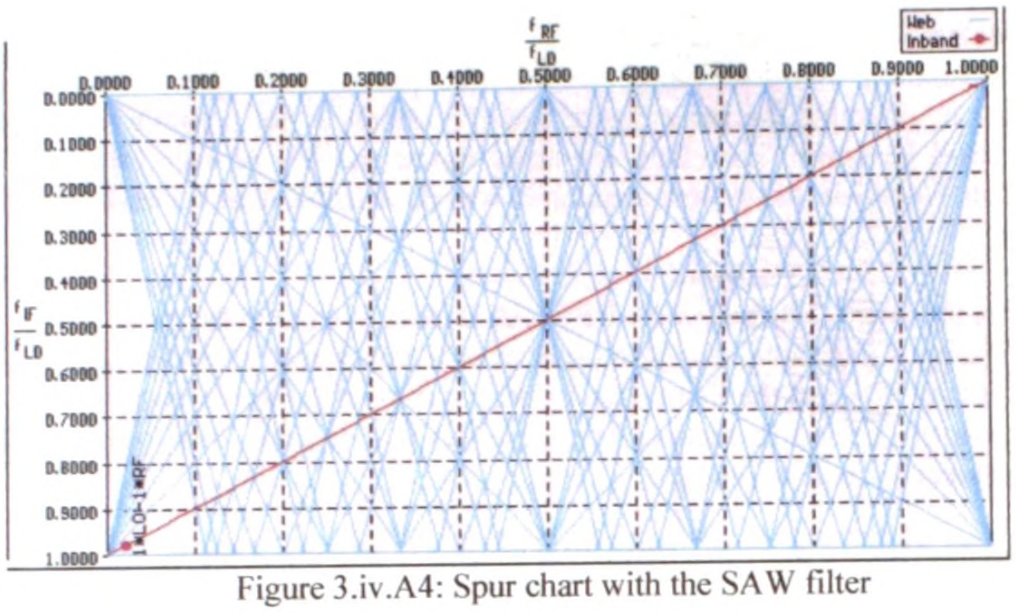

Figure 3.iv.A4: Spur chart with the SAW filter

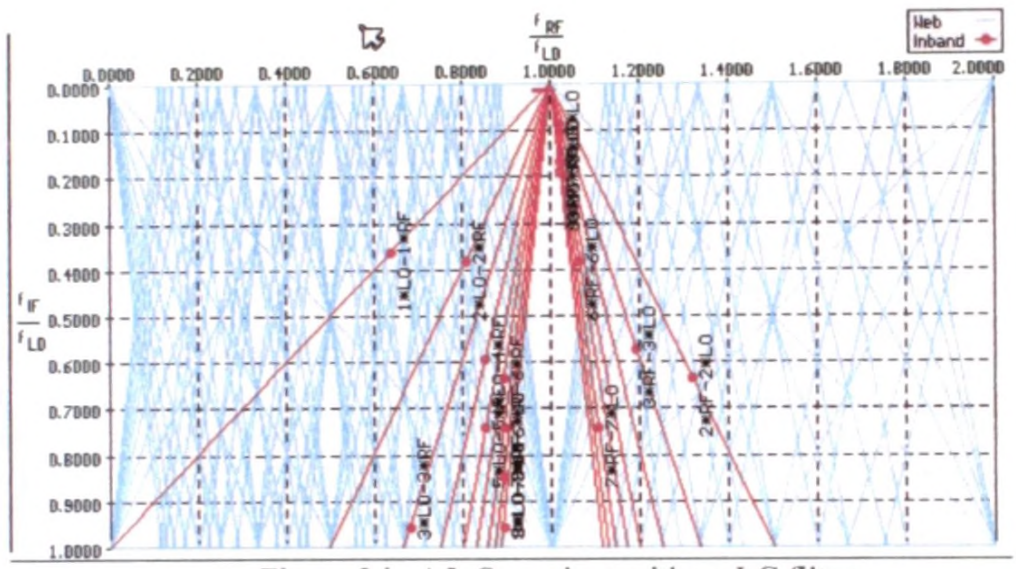

Figure 3.iv.A5: Spur chart with an LC filter

3.iv.A.2 Overall system planning

In the previous section, we decided the frequency plan. Basically, we finalized the frequencies to be used as intermediate frequencies, the oscillator frequencies, and filter specifications. In this section, we go one step further by specifying the gain, noise figure, and nonlinear specifications (IP3 and 1 dB compression points) required to obtain the desired performance. We have already specified our design objectives in Table 3.(iv0.A1. In the next section, we calculate the key design parameters (overall noise figure and IP3) of the system required to meet the design objectives given in Table 3.iv.A1.

3.iv. A.2.1 Selection of key design parameters:

The minimum detectable signal (*MDS*) can be defined in many ways; for example in [1] it is defined as 3 dB above the noise floor, and in [2] as 0 dB above the noise floor. Here we use the definition that the *MDS* is 3 dB above the noise floor. Therefore, if we express power in dBm, *MDS* is given by [1], [2],

$$MDS = -174 + 10\log B + F + 3 \qquad \text{..... Eq. 3.iv.A(2)}$$

where F is the system noise figure in dB. Therefore, if we target the *MDS* to be -110 dBm at an I.F. bandwidth of 200 kHz, then $F \approx 8$ dB. Note that the *MDS* above is measured at the input.

Spurious free dynamic range is given by [1], [2],

$$DR_{sf} = \tfrac{2}{3}(IIP_3 - MDS) \qquad \text{..... Eq. 3.iv.A(3)}$$

where IIP_3 is the third order intercept point referred to the input. Therefore, to achieve the specified spurious free dynamic range of 70 dB, the system IIP_3 should be -5 dBm at the input. In summary, the design targets of section 1 can be achieved with an over all IIP_3 of -5 dBm at the input and a noise figure of 8 dB.

3.iv.A.3 Detailed design of individual stages

The overall system planning was done using the freeware package, RF Work Bench. The RF work bench provides an interface to optimize the noise figure and IP3 which is not possible with even high end design software such as Ansoft Designer. Therefore, the noise figure and IP3 of each individual stage was decided using RF Work Bench. However, the system simulation was done using Ansoft Designer V3.5 to obtain the best simulation accuracy.

Figure 3.iv.A6 shows the results obtained with RF Work Bench. We particularly use RF Work Bench to obtain the IP3 and noise figures of individual stages in order to achieve an over all noise figure of 8 dB or less and an over all IP3 of -5 dBm or better at the input. Bandwidths and intermediate frequencies (IF) of each stage were selected to be the values decided in section 3.iv.A.1. This is to ensure, that there are no harmful spurious products within the dynamic range of interest.

In receiver or transmitter design, there is a trade of between IP3 and the noise figure. Low noise figure requires that substantial amount of gain be present as close to the input as possible. High IP3 requires the opposite: that is as little gain as possible at the input. Therefore, the design involves balancing these two quantities to achieve design targets (in our case N.F.= 8 dB and IP3=-5dB) with components available in the market.

As you can see from Figure 3.iv.A6, we have achieved an over all noise figure of 7.0286 dB meeting the requirement that the it should be less than or equal to 8 dB. Overall IP3 referred to the output is 22.61 dBm. As the over all system gain is 26.4dB (14.6+6.8+5), IP3 at the input (IIP3) is -3.79 dBm. Again, we are well within the criteria that the overall IIP3 should be greater that -5 dBm.

Note, when balancing the over all budget involving the noise figure and IP3, we selected the IP3, noise figure, and gain of each individual stages considering the specifications of components available for fabrication. These details are discussed next.

3.4.A.3.1 Design of Stage 1:

Initial design with RF work bench:

Stage 1 is the most demanding stage in our design. As it can be seen in the over all plan shown in Figure 3.iv.A6, the first stage should have a gain of 14.6 dB, a maximum noise figure of 6.6, and a minimum IP3 of 21.2 dBm referred to the output of the stage[3]. RF Work Bench simulation results of this stage are shown in Figure 3.4.A7. Results show that we get a gain of 14.6 dB, a noise figure of 6.61 dB and an IP3 of 21.3 dBm meeting the design criteria.

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[3] Note, the IP3 values used in all RF Work Bench simulations are the values referred to the output side.

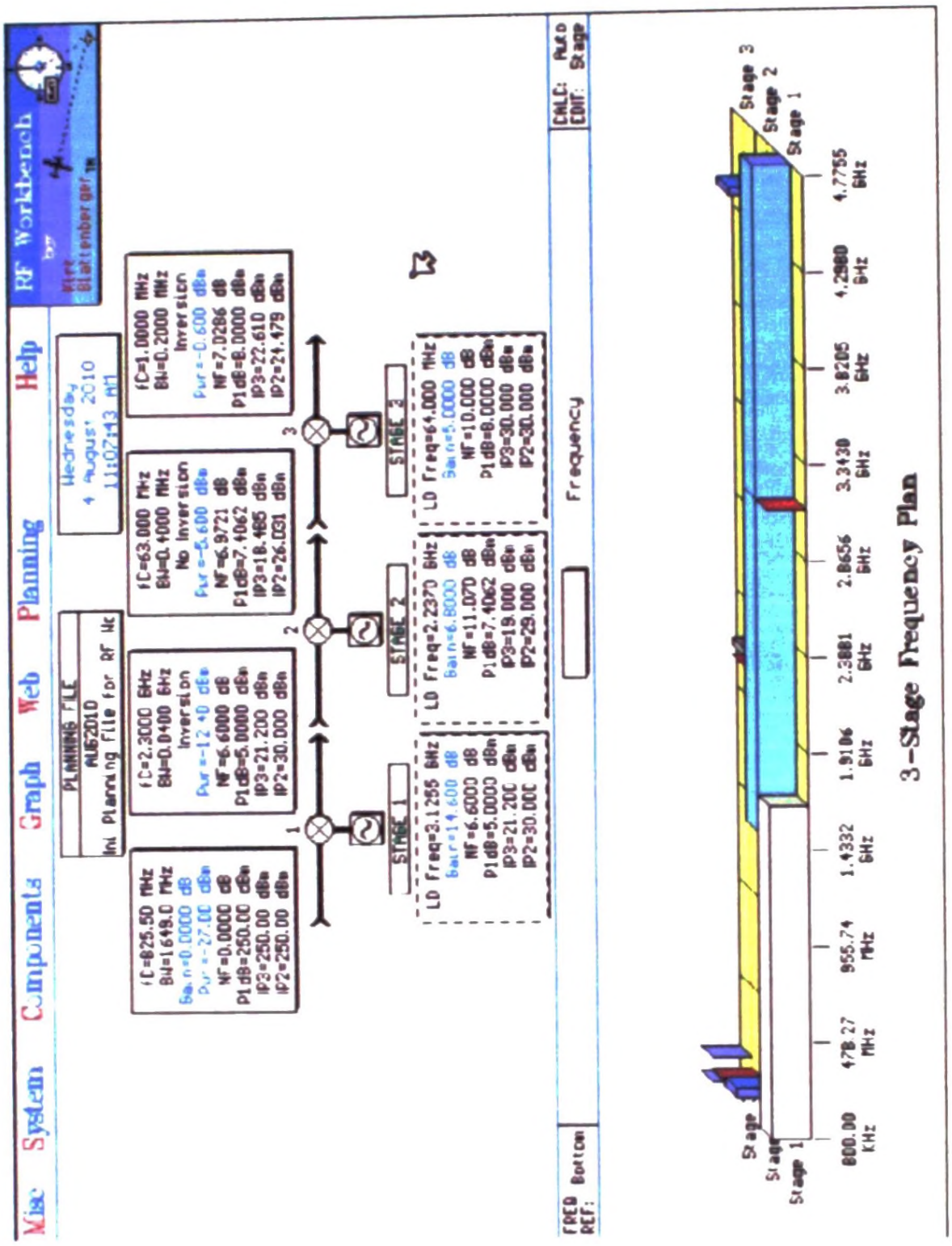


Figure 3.iv.A6: The system plan

We achieve this with the combination of components listed in Table 3.iv.A4. The mixer selected for this stage is SIM-U742MH manufactured by MiniCircuits. As the selected mixer is double-balanced, our selection has an additional advantage of suppressing all even order harmonics of the local oscillator. We have two gain blocks, one prior to the mixer and another after the mixer. The function of the gain block prior to the mixer is to counter the increase of noise figure due to the conversion loss of the mixer. The gain block after the mixer is mainly to isolate the reflections from the IF filter.

The filter stage, prior to the mixer (ie. the pre-selector) is a low pass filter with a cut-off frequency of 1650 MHz and a maximum pass-band insertion loss of 1 dB. The IF filter is a bandpass filter with a centre frequency of 2300 MHz, a bandwidth of 40 MHz and a maximum passband insertion loss of 1 dB. The local oscillator is either DCYS200400-5 from Synergy Corporation or ROS-3360 from MiniCircuits.

The former selection gives a measurement range up to 1700 MHz and the latter selection gives the measurement capability up to 1060 MHz. The actual implementation will have several additional components, for example filters in the LO arm to suppress LO harmonics, an amplifier stage to enhance the LO level, and the biasing circuitry of amplifier stages. These are not discussed in this section as they do not affect the system level design.

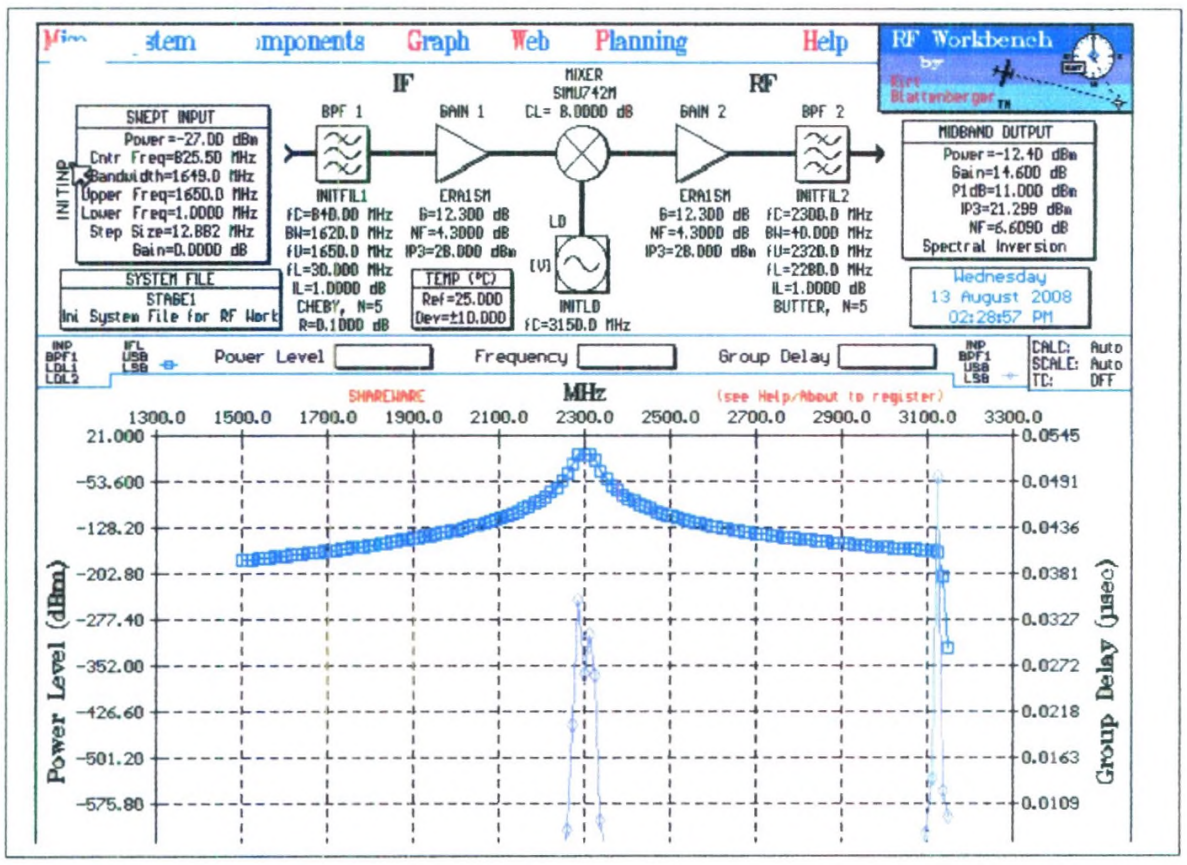


Figure 3.iv.A7: RF Workbench simulation of stage 1

Component	Manufacturer	Model	Specifications
Mixer	MiniCircuits	SIM-U742MH	Con. Loss=8 dB, IIP3=20 dB, Input:0.1-3300MHz, output: 2300-7400 MHz. LO: 2300-7400
VCO	Synergy	DCYS-200400-5	Freq: 2000-4000 MHz,
VCO	MiniCircuits	ROS-3360	Freq: 2120-3360 MHz, Power supply=12V, power out=8.5 dBm
LNA	MiniCircuits	ERA-1SM	Freq: DC-8000 MHz, Max Gain=12.3 dB, NF=4.3dB, OIP3=28 dBm.
IF Amp	MiniCircuits	ERA-1SM	Freq: DC-8000 MHz, Max Gain=12.3 dB, NF=4.3dB, OIP3=28 dBm.
Pre-selector	Designed and fabricated		Lowpass filter with cut-off freq=1650 (or 1060), and passband IL less than 1 dB.
IF filter	Designed and fabricated		Bandpass filter: Center freq=2300 MHz, BW=40 MHz, passband IL less than 1 dB.

Table 3.iv.A4: Key components used in stage 1

Simulation and layout design of stage 1 using Ansoft Designer V3.5:

In this section, we refine the results obtained in the previous section using Ansoft Designer. The schematic diagram used for the simulation is shown in Figure 3.iv.A8. The Ansoft Designer based simulation is more accurate due to the following reasons.

- The effects due to interconnection traces are taken into account. These effects are significant at microwave frequencies.
- The effects due to the biasing circuits are included.

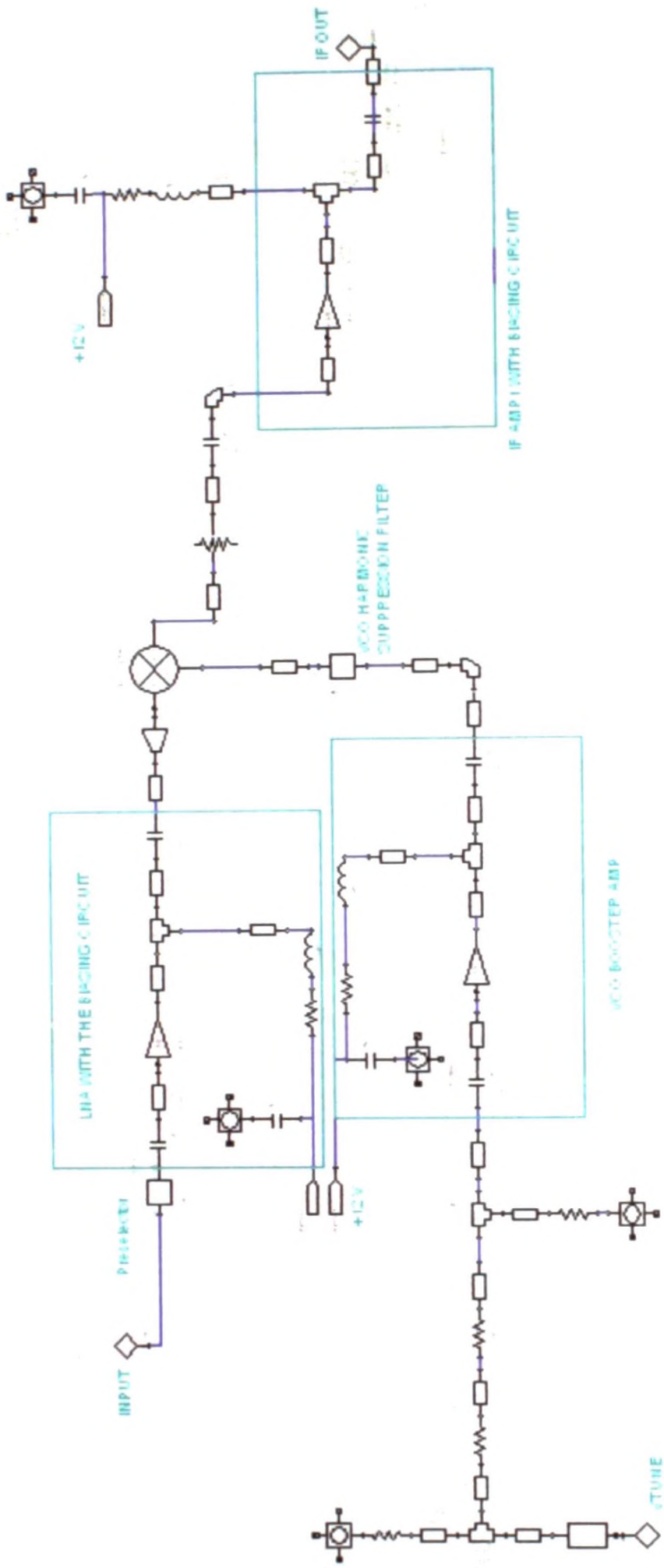


Figure 3.iv.A8: Schematic diagram of stage 1

- Components used are characterized by complete s-parameter files. For example, in the RF Workbench simulation, we characterize the ERA-1SM amplifiers by gain, noise figure, and IP3. In this simulation we use the scattering parameter table provided by the manufacturer which specifies 2-port scattering parameter values from 50 MHz to 11 GHz.

In addition, we use Ansoft Designer to generate the layout diagrams. Results obtained at various levels of simulation with Ansoft Designer are illustrated in Figure 3.iv.A.9 to Figure 3.iv.A.14.

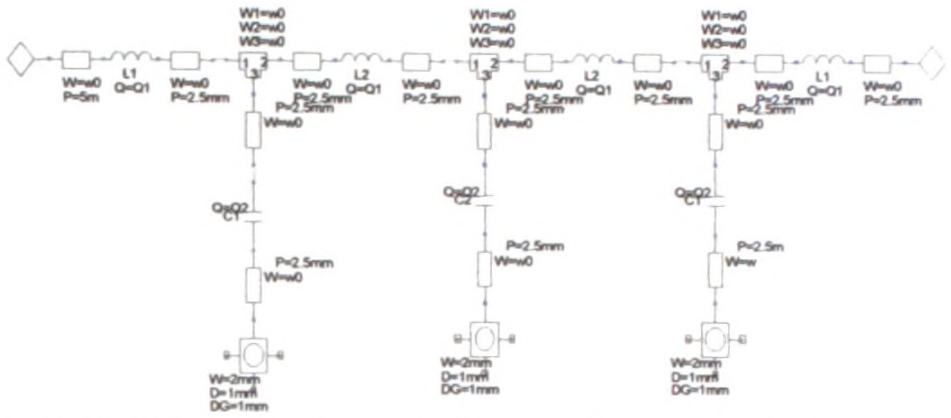


Figure 3.iv.A9: Schematic diagram of the pre-selector of the first stage

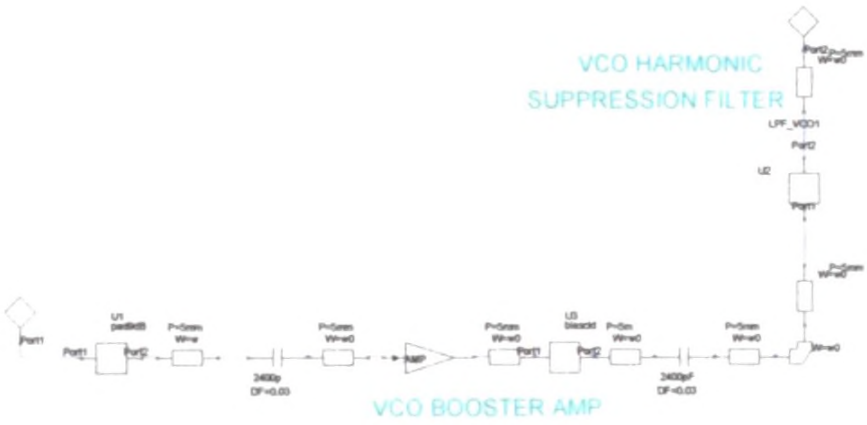


Figure 3.iv.A10: VCO arm simulation

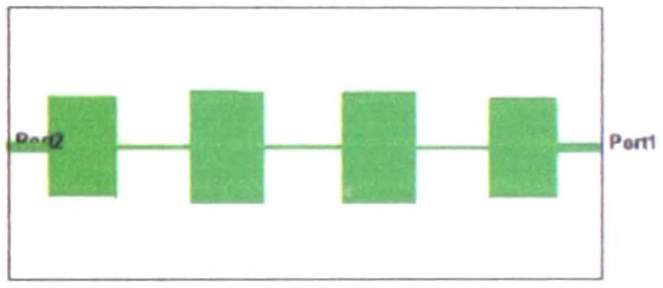
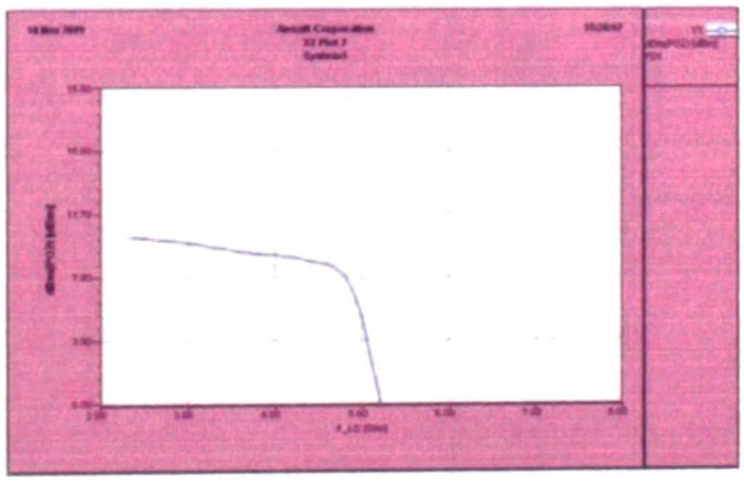
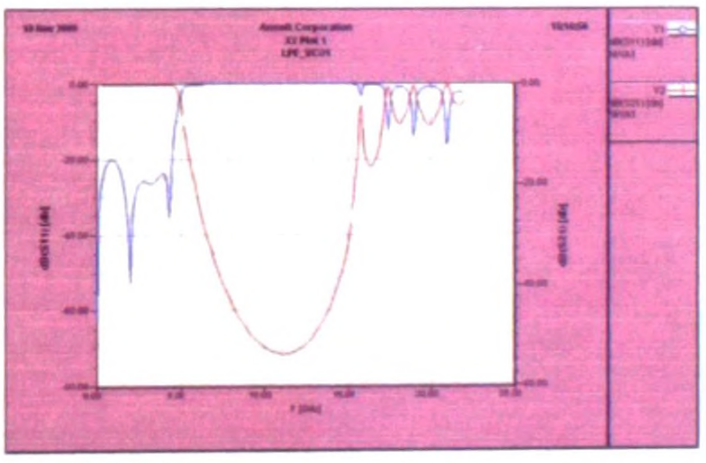


Figure 3.iv.A11: Layout of the VCO filter of stage 1

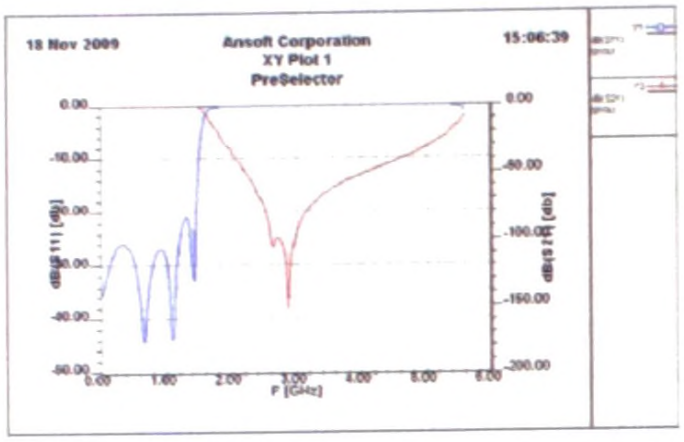


(a) Simulation results of the VCO arm

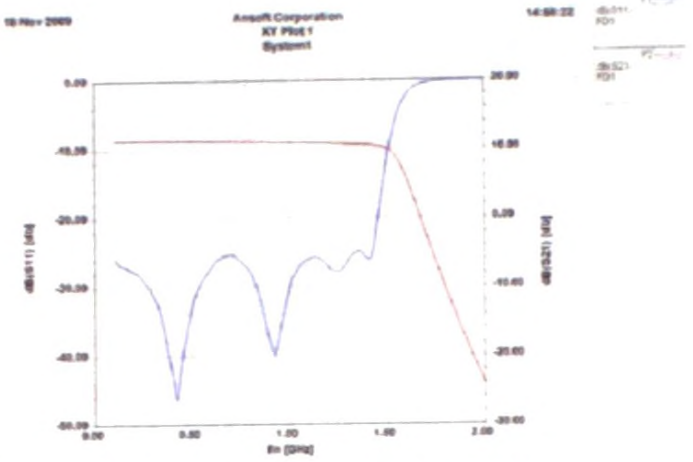


(b) Response of the VCO filter of stage 1

Figure 3.iv.A12:



(a) Response of the pre-selector of stage 1



(b) Tuning response of stage 1

Figure 3.iv.A13

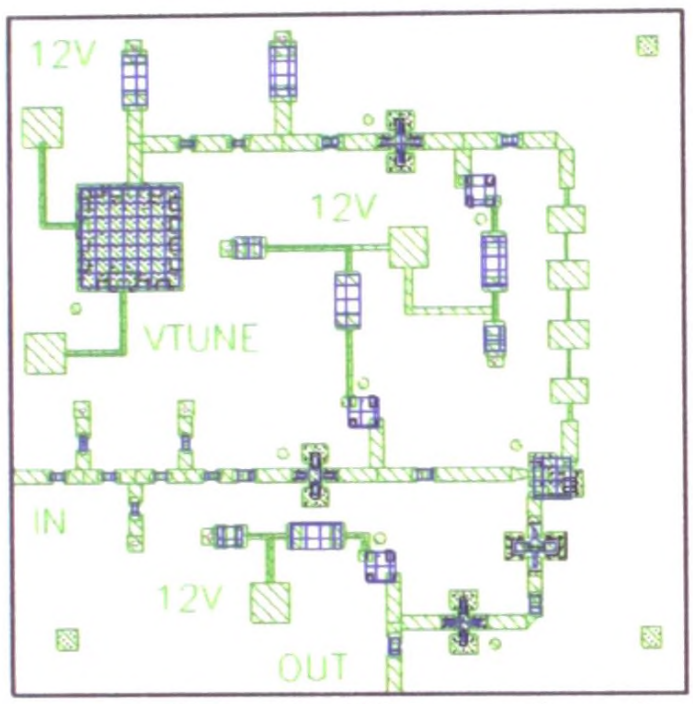


Figure 3.iv.A14: Layout of stage 1

Design of the first I.F. filter:

This is a bandpass filter with a centre frequency of 2300 MHz and a bandwidth of 40 MHz. The required fractional bandwidth is 1.7 %. We also target for a passband insertion loss less than 1 dB and a return loss greater than 20 dB. As the second I.F. frequency is 64 MHz, the image frequency is at 2364. We set the image suppression to 80 dB. Therefore, the specifications of the 1st I.F. filter can be summarized as shown in Table 3.iv.A5.

Pass band center frequency/MHz	Bandwidth/ MHz	Passband insertion loss/ dB	Passband return loss/dB	Attenuation at 2364 MHz
2300	40	1	20	80

Table 3.iv.A5: Specification of the first I.F. Filter.

From classical filter theory it can be shown that the above specifications can be met with a 7th order Chebyshev filter with a passband ripple of 0.036 dB. We implement this filter as a micro-strip inter-digital filter. The design of this type of filters is described in [7] and [8]. Once the filter order and the ripple are known, the element values of the corresponding low-pass filter prototype can be found either using formulas or filter tables. We use the filter table published in [8]. For a 7th order Chebyshev filter with a passband ripple of 0.036 dB, the element values are given below.

$$g_0 = g_8 = 1.0000, \quad g_1 = g_7 = 0.9763,$$

$$g_2 = g_6 = 1.4353\ , \quad g_3 = g_5 = 1.9115\ , \quad g_4 = 1.6278$$

From these prototype element values, the coupling coefficients between resonators ($K_{i,i+1}$) and Q_{ex}values can be calculate using the following formulas [8]:

$$K_{i,i+1} = {B}/{\sqrt{g_i g_{i+1}}} \quad \text{..... Eq3.iv.A(4)}$$

$$Q_{ex1} = {g_0 g_1}/{B} \quad \text{..... Eq3.iv.A(5)}$$

$$Q_{exN} = {g_N g_{N+1}}/{B} \quad \text{.....Eq3.iv.A(6)}$$

where N is the filter order and B is the fractional bandwidth. Once the coupling coefficients and Q_{ex} values are found, all we need is to find out the dimensions required to obtain desired $K_{i,i+1}$ and Q_{ex} values. Until recent times, this was done by fabricating number of test circuits with different dimensions and measuring the coupling coefficients and external Q values [7]. However, with new developments in accurate simulation software, it is now possible to perform these experiments using computer simulation [8]. This is the method followed in our design.

In Figure 3.iv.A15, we model two micro-strip lines separated by a known distance (60 mil in Figure 3.iv.A15). From the double resonance peaks of the resulting response, the coupling coefficient is calculated as follows:

$$K = \frac{f_{high} - f_{low}}{f_0} \quad \text{.....Eq3.iv.A(7)}$$

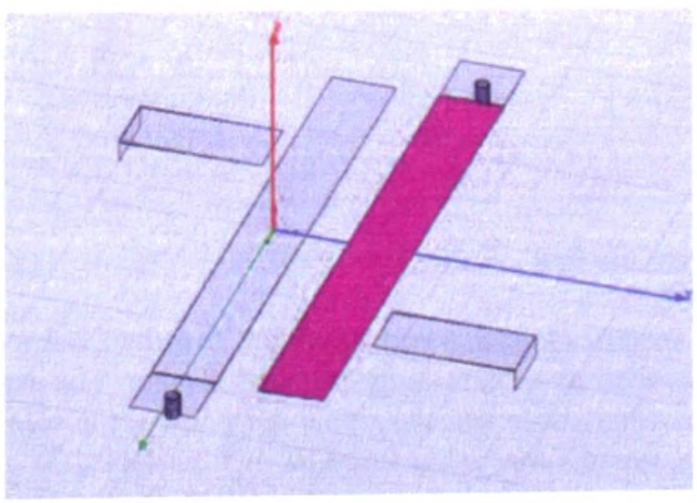
where $f_{high}$is the frequency of the upper peak and f_{low} is the frequency of the lower peak. f_0 is the design frequency, and in our case it is 2300 MHz. The design curve shown in Figure 3.iv.A17 (a) was obtained this way.

Similarly, to find the optimum tap position, we modeled a tapped micro-strip line as shown in 3.iv.A16. In [8] it is shown that the reflected time delay t_d is related to Q_{ex} as shown in the equation below.

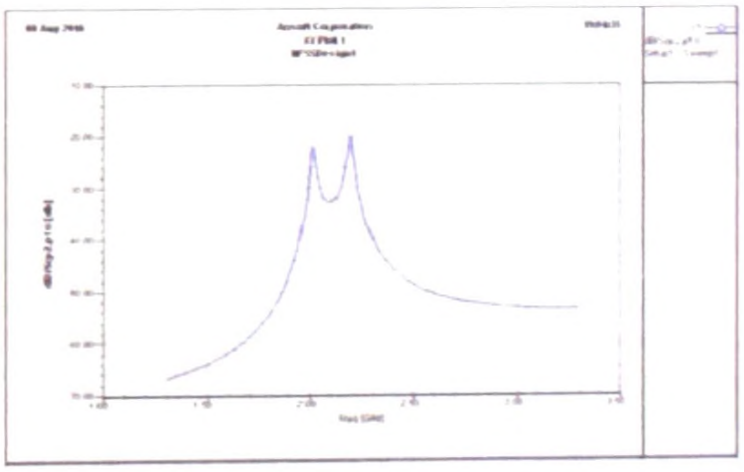
$$Q_{ex} = \frac{\pi f_o t_d}{2} \quad \text{.....Eq3.iv.A(8)}$$

The design curve for the optimum tap position (Figure 3.iv.A17 (b)) was obtained by carrying out a number of simulations with different tap positions.

Once the design curves are obtained, the dimensions of the filter can be directly read from the design curves as we have already calculated $K$and Q_{ex} values. The complete filter with these dimensions was then simulated as shown in Figure 3.iv.A18.

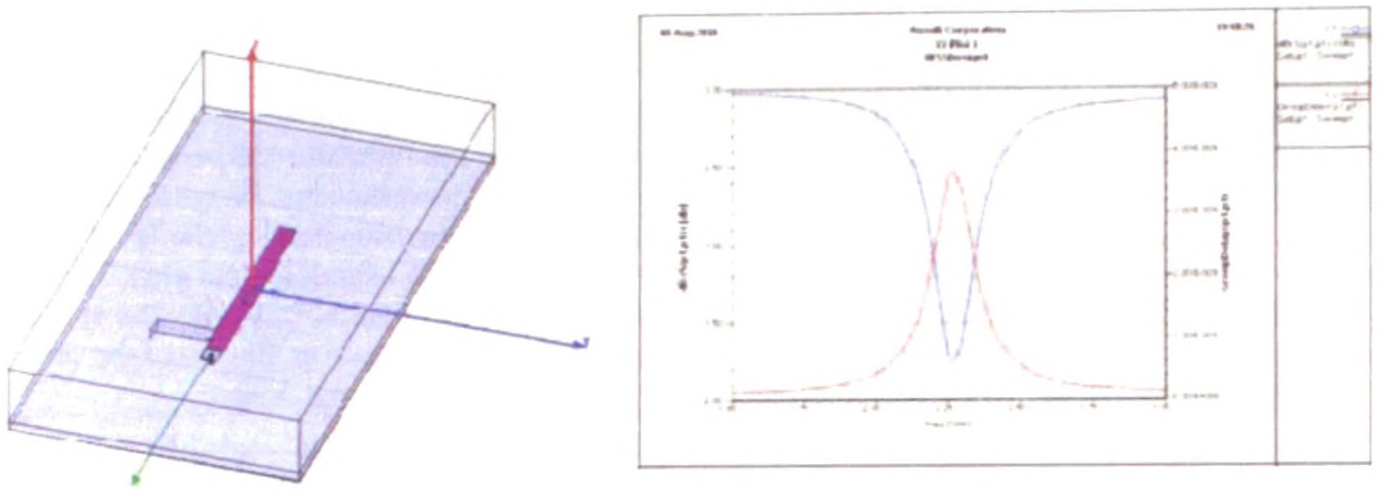


(a) HFSS Model



(b) Double resonance response with a strip separation of 60 mil.

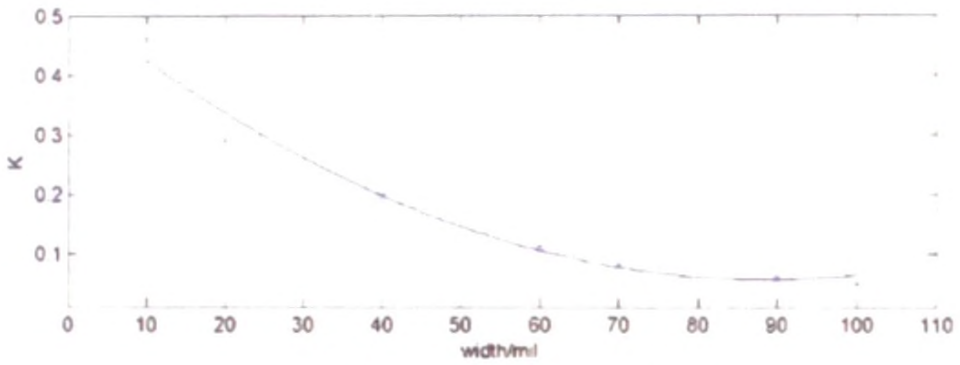
Figure 3.iv.A15: Experiment to find out the variation of $K$with line spacing



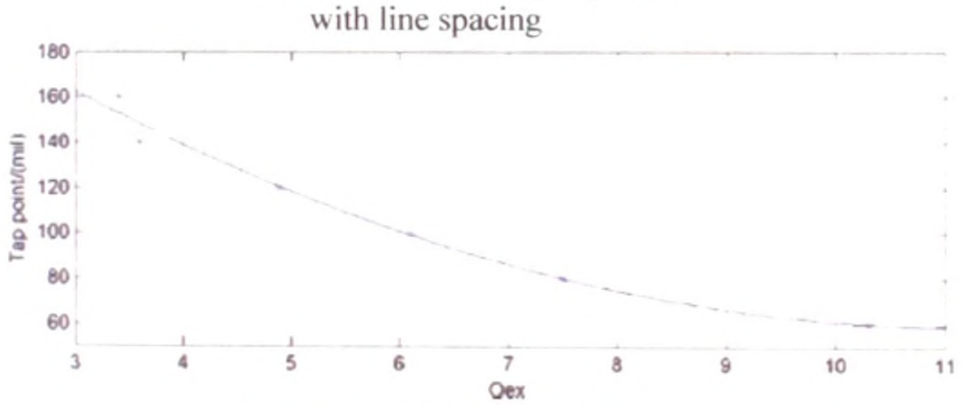
(a) HFSS Model

(b) Group delay and reflection coefficient variation.

Figure 3.iv.A16: Experiment to find the optimum tap position.



(a) Variation of coupling factor with line spacing



(b) Variation of external Q with tap position.

Figure 3.iv.A17: Design curves

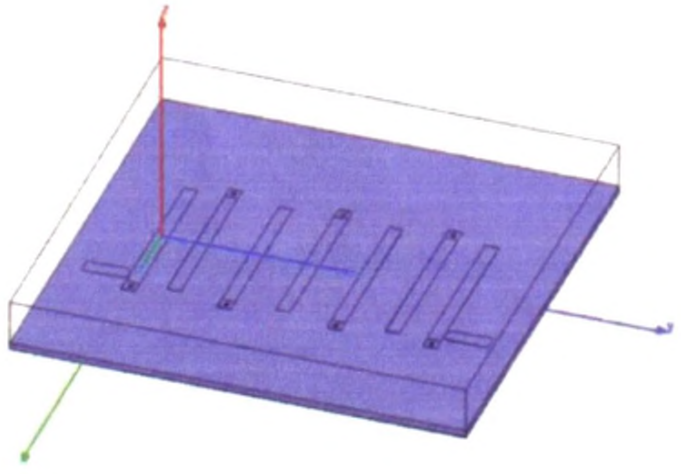


Figure 3.iv.A.18: HFSS model of the inter-digital filter

3.iv.A.3.2 Design of Stage 2:

Initial design with RF Workbench:

Key components used in Stage 2 are listed in Table 3.iv.A6. The system performance when these components are used is shown in Figure 3.iv.A19. Note that in this simulation, the filter and the pre-amplifier prior to the mixer are dummy stages. That is, in practice, the 2nd mixer is directly connected to the output of the 1st IF filter. We use a gain block after the mixer to suppress the reflections from the stop-band of the IF filter entering the mixer. As it can be seen, stage 2 also satisfies the design objectives of the overall system plan. The gain of stage 2 is 6.8 dB. Noise figure of 1st and second stage combination is less than 6.9721 dB. The IP3 of the same combination is greater than 18.485 dBm referred to the output. Note, that the over all gain of the stage is exactly 6.8 dB for an I.F. filter with a 15 dB insertion loss, the SAW filter we used in the design.

Component	Manufacturer	Model	Specifications
Mixer	MiniCircuits	MBA-15LH	Conv. Loss = 5.6 (Typ.), IP3=15 dBm, Input/LO: 1200-2400 MHz, IF=DC-600 MHz.
IF Amp	MiniCircuits	HELA-10D	Gain=11 dB (Typ.), NF=3.5 dB, IP3=48 dBm, Freq: 8-300 MHz.
IF Filter	Sawcom Tech, Inc., U.S.A.	Part No: 063004	Bandpass SAW filter. Centre freq = 63 MHz, BW=400 kHz. Passband IL=15 dB.
Local Oscillator	MiniCircuits	ROS2252C	Freq: 2103-2252 MHz, Output=-1dBm

Table 3.iv.A6: Key components used in Stage 2

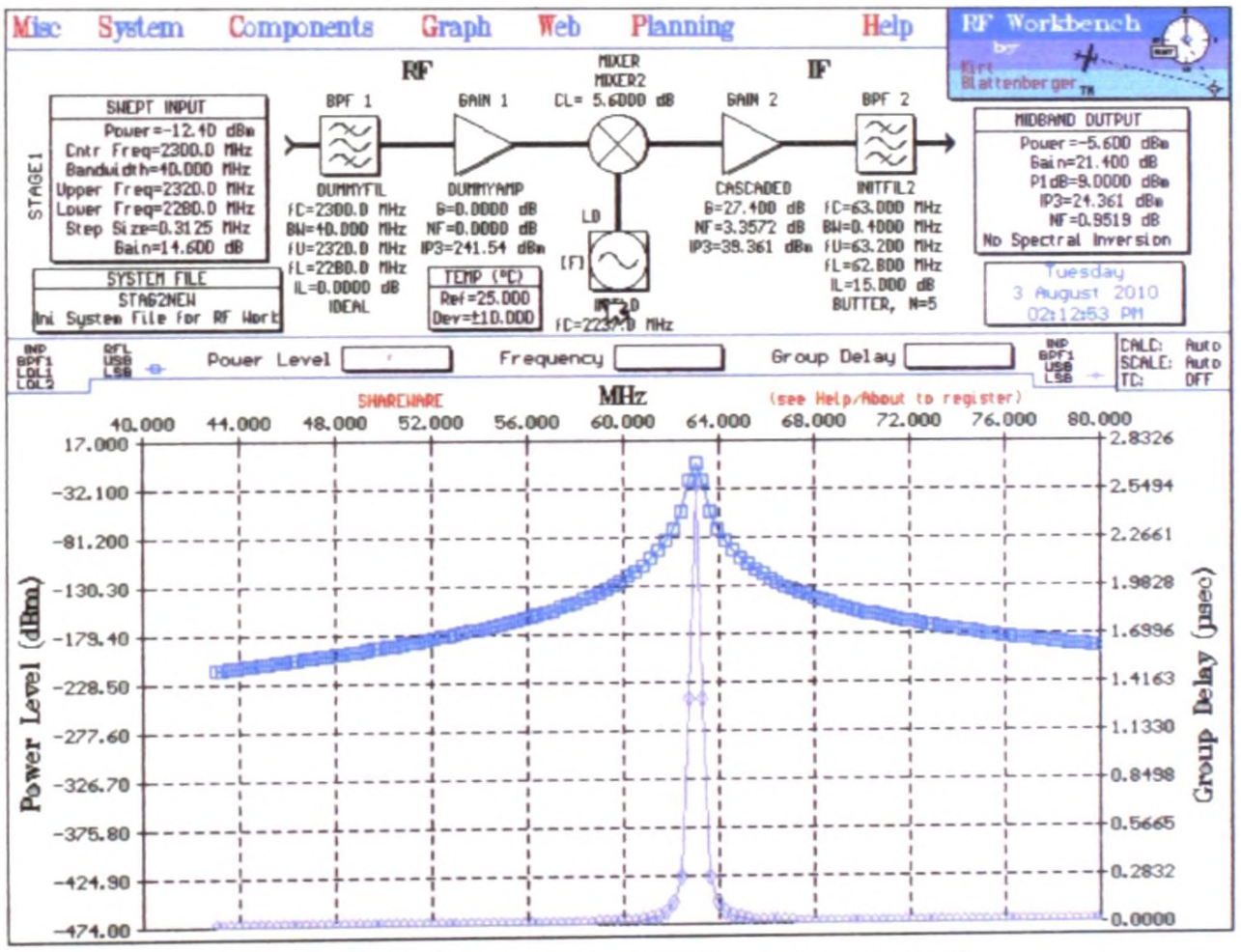


Figure 3.iv.A19: RF workbench simulation of stage 2

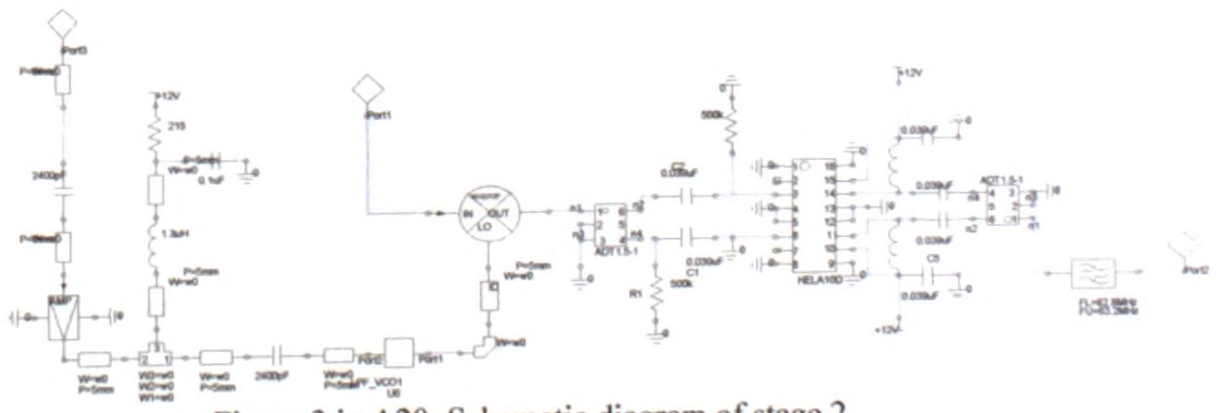


Figure 3.iv.A20: Schematic diagram of stage 2

Simulation and layout design of stage 2 using Ansoft Designer V3.5:

Figure 3.iv.A20 shows the schematic diagram used for the Ansoft Designer simulation. The simulated conversion gain is shown in Figure 3.iv.A21. Note the steep cutoff characteristics due to the SAW filter used. The layout generated using Ansoft Designer is shown in Figure 3.iv.22.

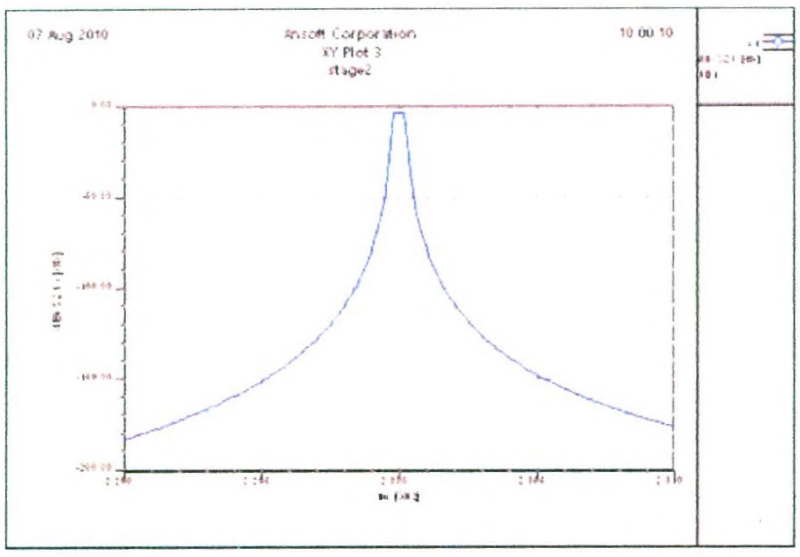


Figure 3.iv.A21: Conversion gain of stage 2

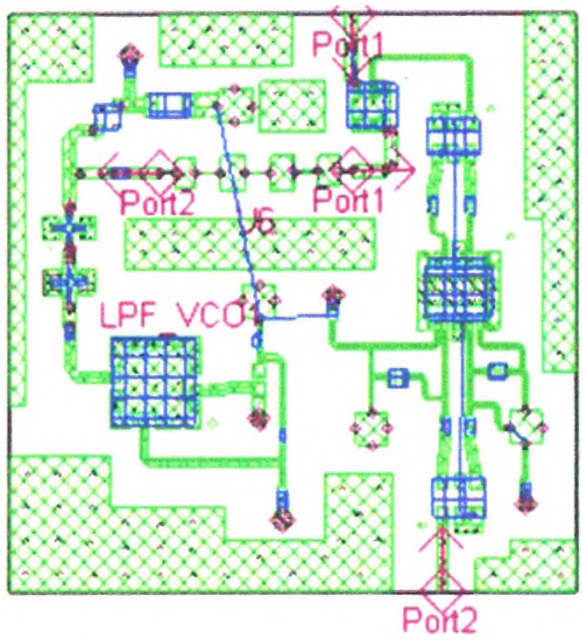


Figure 3.iv.A22: Layout of stage 2

3.iv.A.3.3 Design of Stage 3:

Figure 3.iv.A23 shows the system analysis of this stage obtained with RF Work Bench. All stages prior to the mixer are dummy stages. Amplifier following the mixer is for reducing the any reflections in the stop-band of the IF filter entering the mixer

As in the previous stages, we can see that our design objectives, the noise factor and IP3 at the end of stage 3 are satisfied. In section 3.iv.A.2.1 we selected the overall noise figure to be less than 8 dB and IP3 referred to the input to be larger than -5 dBm. Figure A.3.iv.23 shows what we get, a noise figure of 7.0419 dB and an IIP3 of -4.73 dBm (ie., 26.27 – 31).

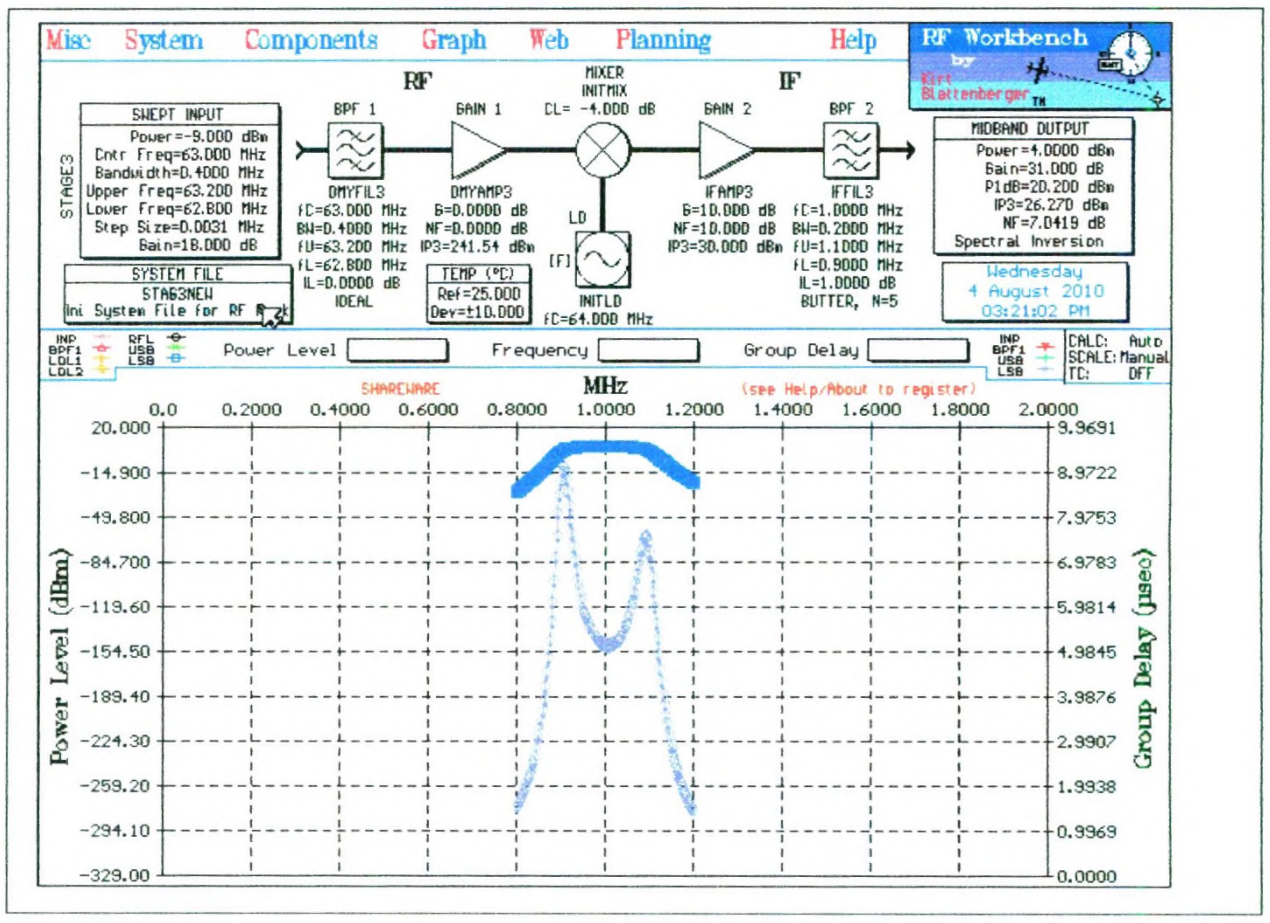


Figure 3.iv.A23: RF Workbench simulation of stage 3

Detailed Design of Stage 3 using Ansoft Designer V3.5:
As it is already emphasized in previous sections, in this stage, the signal is down converted from 63 MHz to 1 MHz. Therefore, this is purely a RF circuit design. We describe the details of the key segments of stage 3, namely, the local oscillator, mixer, and amplifier stages next.

Design of the Local Oscillator
The selected topology is a common-base overtone oscillator which uses a series mode crystal for stability. The schematic diagram of the oscillator is given in Figure 3.4.A24 below.

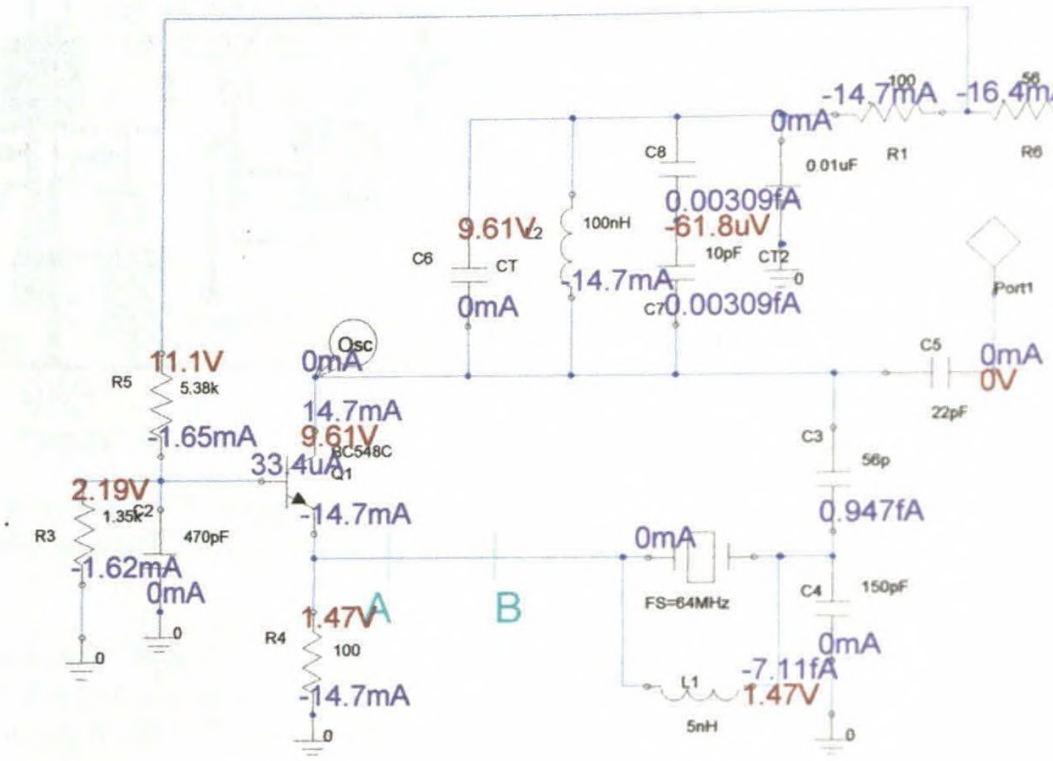


Figure 3.iv.A24: Schematic diagram of the oscillator.

Biasing the transistor:
The transistor selected for the design is BC548 manufactured by FAIRCHILD Semiconductors. Our choice is motivated by the fact that this transistor is economical, widely available, and has a unity gain frequency, f_t, of 300 MHz[4]. We select $V_{CE} = 8V$ and $I_C = 15\text{mA}$ as the biasing point.

Supply voltage, V_{CC} is selected to be 12 V as this supply voltage is used in other stages (stage 1 and stage 2). We begin the bias calculation by setting the emitter voltage to 1.5 V. Note that $V_{CE} = 8$ V. If we assume, $\beta \cong 100$, this implies that $R4$ has to be 99 Ω. So, we select 100 Ω as $R4$. Now, $V_B = 2.1\text{V}$ and $V_C = 9.5\text{V}$. We select $R1$ (the collector resistor) to be equal to $R4$ (the emitter resistor) to make the calculations simple. As a result, the potential at the node that connects $R5$, $R6$, and $R1$ becomes 11V (Note, the collector current is 15 mA).

Assuming $V_{BE} = 0.6$ V, we attempt to set the base voltage to 2.1 V. If we assume $\beta \cong 100$, the base current becomes 0.15 mA. Thus, if we stick to the rule of thumb that the current in the potential divider arm should be at least 10 times the base current, we end up with $R3 = 1.35$ k and $R5 = 5.38$ k. Finally, $R6$ is selected to be 56 Ω to give a 1 V potential difference across it when the current through the resistor ($R6$) is 16.5 mA (ie. 15 mA plus 1.5 mA in the potential divider arm). Figure 3.(iv).A24 shows the resulting biasing conditions obtained with a dc bias analysis using Ansoft Designer V3.5. It can be seen that the resulting bias voltages and currents are within 2% of the expected values.

[4] Note that f_t should be much higher than the design frequency (64 MHz in our case), and selecting a factor of 5 is standard practice [2].

Design of the resonant circuit:
The resonant circuit comprises the capacitors C3, C4, and the inductor L2. Later we add the capacitors C6, C7, and C8 for tuning. The values selected for C3 and C4 are 56 pF and 150 pF. The resonant frequency of the circuit, f_0, is given by

$$2\pi f_0 = \sqrt{\frac{C_3 + C_4}{L_2 C_3 C_4}}$$

Therefore, the circuit resonates at 64 MHz when $L_2 = 189\ nH$. We selected 100 nH for $L_2$and the circuit was tuned to 64 MHz using the trimmer capacitors C6 and C7. The 470 pF capacitor (C2) at the base grounds the base for RF signals.

Performance verification with simulations
To ensure that the circuit oscillates, we verify if the Barkhausen criteria [5] is satisfied. We open the positive feedback loop at points A and B (see Figure 3.iv.A25) and the Bode plot was obtained. The results are shown in Figure 3.iv.A21. The plot clearly shows that the phase angle (red curve) is zero at 64 MHz and has a gain margin of about 10 dB ensuring that there will not be any start-up problems. Figure 3.iv.A26 shows the output power spectrum of the oscillator obtained with a non-linear analysis technique, harmonic balance analysis to be specific. We examined harmonic levels up to the 7th harmonic as shown in the figure. Note that the desired output level is more than +15 dBm while the highest harmonic level (2nd harmonic in this case) is more than 20 dB below.

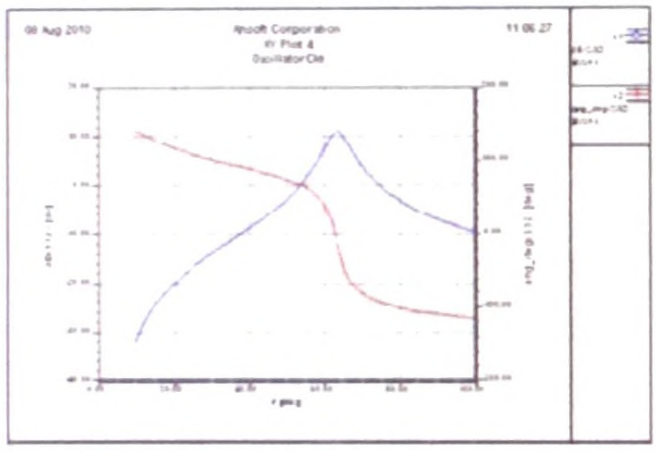


Figure 3.iv.A25: Open loop simulation of the oscillator

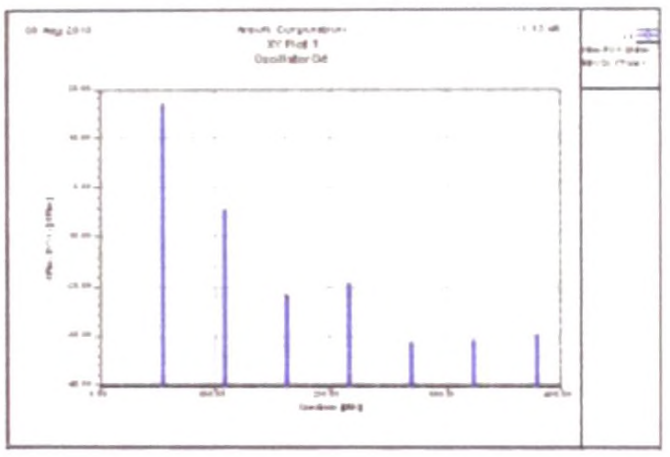


Figure 3.iv.A26: Oscillator output obtained by harmonic balance simulation

Design of the 3rd mixer stage:

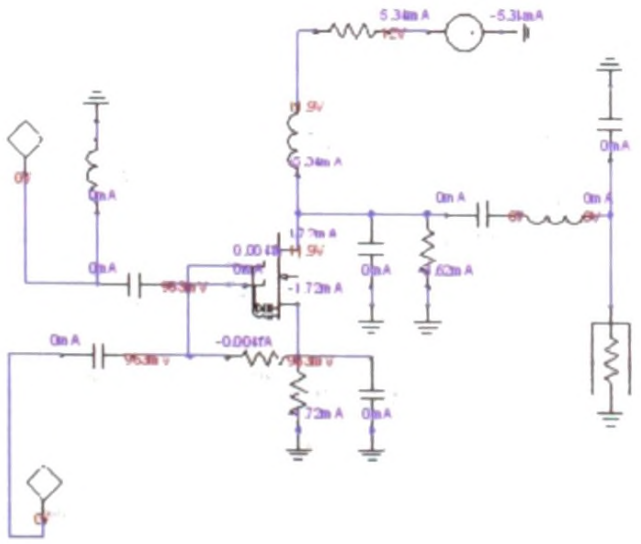
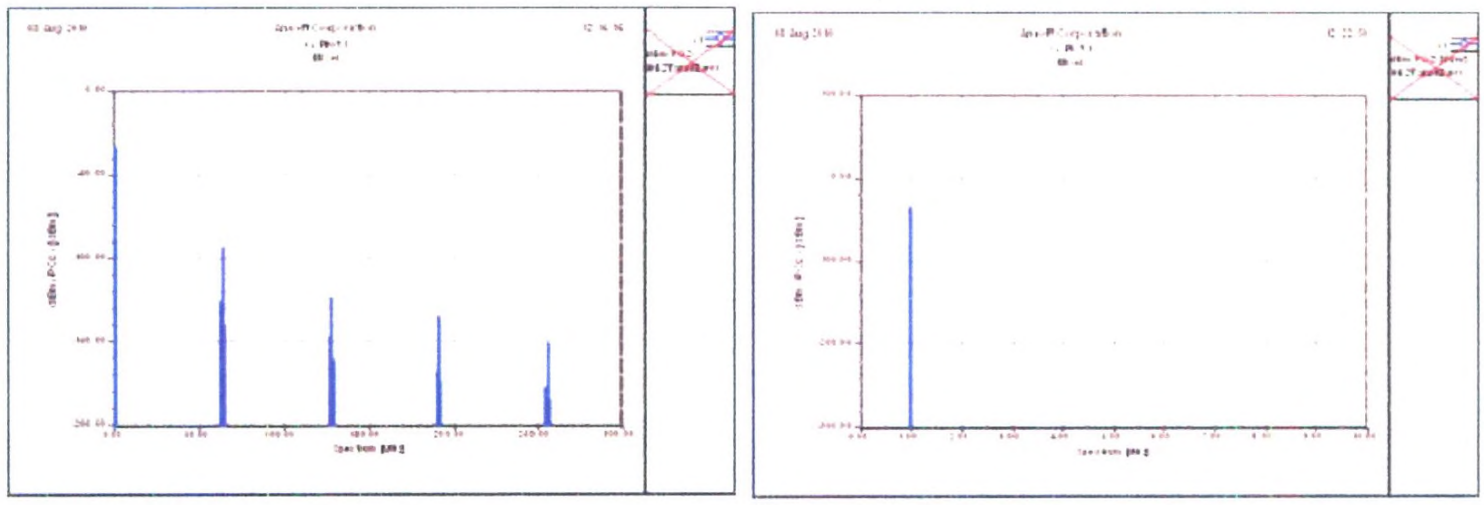


Figure 3.iv.A27 Schematic diagram of the dual gate mixer

The down conversion from 63 MHz to 1 MHz is done by using a dual gate FET mixer circuit. The dual gate FET used for the design is BF981 which is an N-channel depletion type device. We selected a dual gate FET architecture to obtain good isolation between LO and I.F. ports. This circuit is a standard mixer circuit published in literature [2] and therefore we do not discuss the design. However, the circuit was simulated using Ansoft

Designer V3.5 and the results are presented. The biasing conditions are illustrated in Figure 3.iv.A27. The results obtained with a two-tone harmonic balance simulation of the mixer are shown in Figure 3.iv.A28.

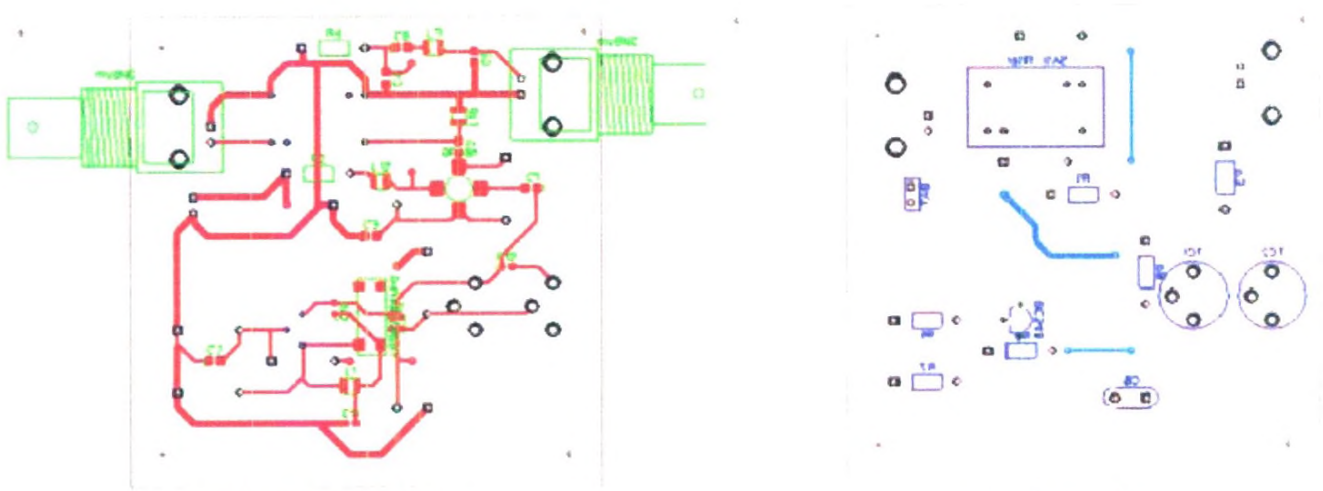


(a) Harmonics and spurs generated

(b) Zoomed image showing the desired tem at 1 MHz.

Figure 3.iv.A28: Harmonic balance simulation of 3rd mixer stage

When fabricating this stage, we do not use ground plane technology as the frequency of operation is below 100 MHz. As components required include both surface mount and through hole types, we fabricated this circuit as an ordinary double sided PCB. For this we used "Diptrace", another free software package available. The layouts generated using Diptrace are shown in Figure 3.iv.A29.



(a) Bottom side

(b) Top side

Figure 3.iv.A29: Layout diagrams of stage 3

3.v. A Results:

The key parameters used in the design are the gain, noise figure or the IP3. Therefore, to verify the performance of the system, we measure these three parameters.

3.v.A.1 The measured performance of stage 1

The image in Figure 3.v.A1 is a photograph of the 1st conversion stage packaged in an Aluminum casing. The circuit is gold plated to protect copper traces/layers. The substrate used for fabricating the circuit is Neltec NX9320, a low loss material used for microwave circuit fabrication. For the RF input and the 2.3 GHz IF, we use panel mounted SMA connectors. Supply and tuning voltages are supplies through feed through capacitors to give a professional finish to the final fabricated circuit.

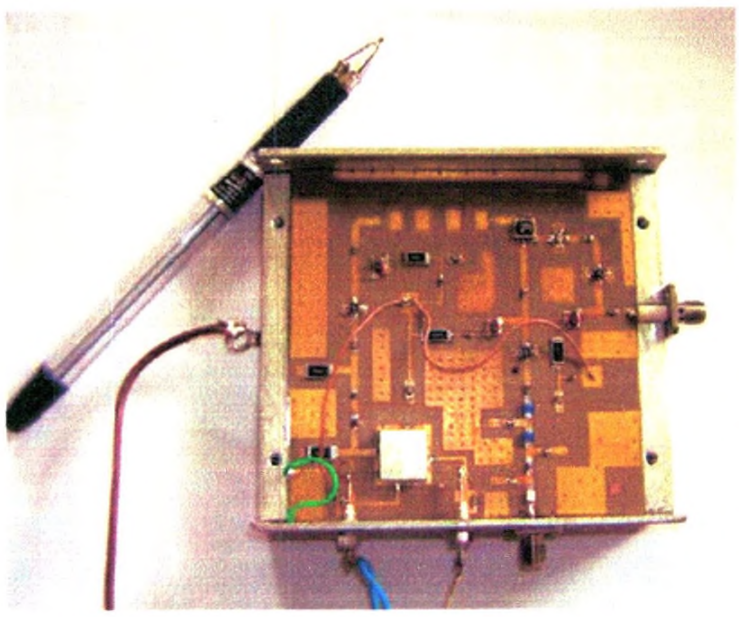


Figure 3.v.A1: Stage 1 completed and packaged

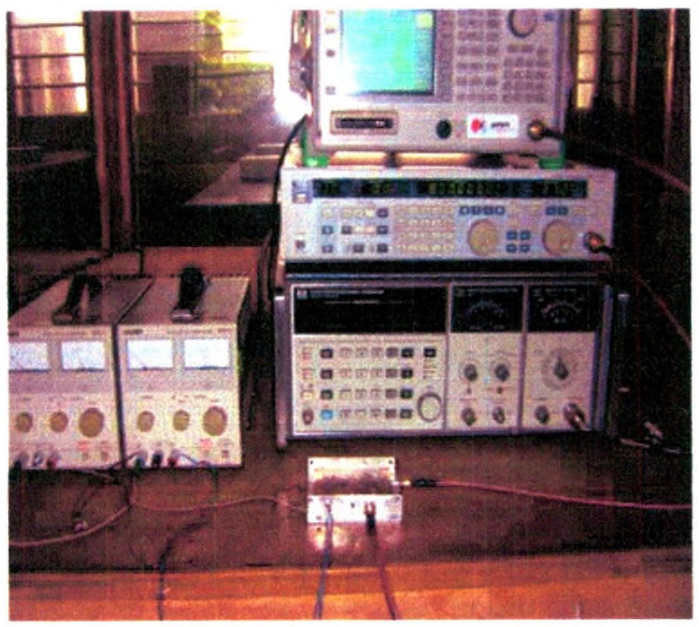


Figure 3.v.A2: Conversion gain measurement of stage 1

3.vA.1.1 Conversion gain measurement of stage 1

We measured the conversion gain using an Agilent Spectrum Analyzer and a Kenwood RF signal synthesizer. Details of the experimental set up is given in Section 3.v.A.4.1 as this is common to the measurements of all three stages. These measurements were made at an input power level of -50 dBm and at the IF frequency of 2.3 GHz. The results are given in Table 3.v.A5.

f_{in}/MHz	Conversion gain of stage 1 /(dB)	
	Measured	Simulated
200	6	11.5
300	6	11.4
400	6	11.4
500	6	11.3
600	6	11.3
700	6	11.2

f_{in}/MHz	Conversion gain of stage 1 /(dB)	
	Measured	Simulated
800	6	11.2
900	5	11.1
1000	4	11.0
1100	3	10.9
1200	2	10.8
1300	2	10.7

Table 3.v.A1: Comparison of measured and simulated gains of stage 1

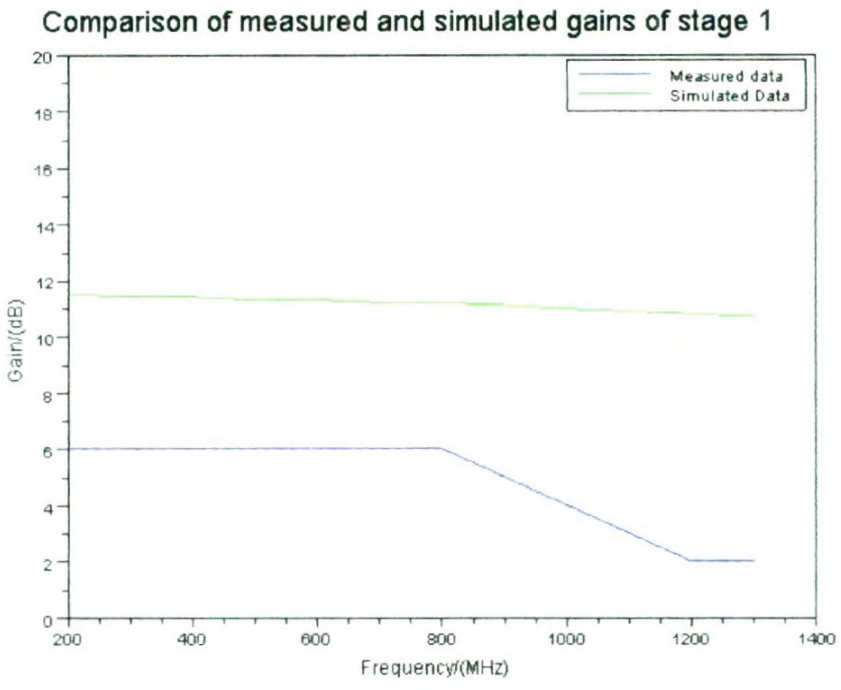


Figure 3.v.A3: Comparison of measured v.s. simulated data

In Figure 3.v.A3, the results are given as a plot for comparison. Although there is a 6 dB difference in gain when compared to the simulations, stage 1 demonstrates a working system. The 6 dB difference could be attributed two reasons. The simulation assumes the insertion loss of the first I.F. filter (2.3 GHz) is less than 1 dB. Such a low insertion loss with a steep cutoff in the GHz range can usually be achieve with a cavity type filter. Due to the limitation of time, we use an edge coupled micro-strip bandpass filter instead of a cavity filter. The microstrip filter has an insertion loss of 12 dB.

The other reason for the difference is the fact that we drive the mixer stage at +10 dBm rather than at +13 dBm, the rated LO power level. We under-drive the mixer as we could not find a LO booster amplifier that can handle +13 dBm in the items ordered.

Although stage 1 is fully functional as it is, its performance can be improved by using a cavity filter for the IF filter and operating the mixer at the rated power.

3.v.A.1.4. Performance measurement of the inter-digital filter

The inter digital filter was fabricated on a 2"x2" Neltec, NX9320 substrate. This is shown in Figure 3.v.A4. Filter characteristics were measured using a microwave network analyzer (see Figure 3.v.A5).

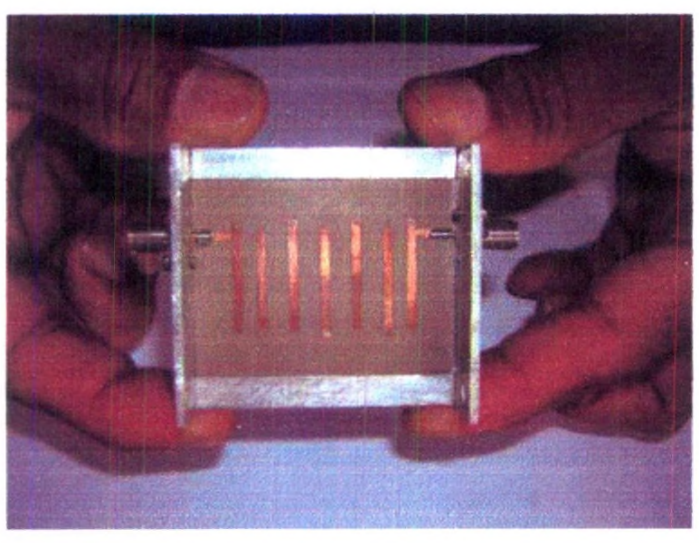


Figure 3.v.A4: Inter-digital filter fabricated on a 2"x2" Neltec NX320 substrate

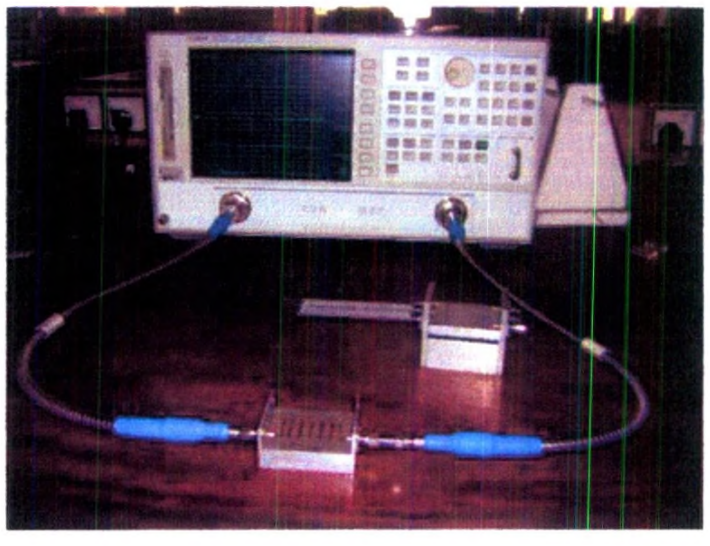


Figure 3.v.A5: Performance measurement with a microwave network analyzer.

The measured results are given in the screen dump shown in Figure 3.v.A6. As the marker indicates, the filter response is centered at 2.178 GHz and has a -17.46 dB insertion loss. We could have tuned the filter to resonate exactly at 2.3 GHz using the technique described in the classic paper by Dishal [6]. However, we do not explore this as the insertion loss is unacceptably high. This was also detected at simulation level (see Figure 3.iv.A??). As it was difficult to figure out the cause for this high insertion loss, we stopped the inter-digital filter at this stage with plans to implement the same filter using resonant cavity technology.

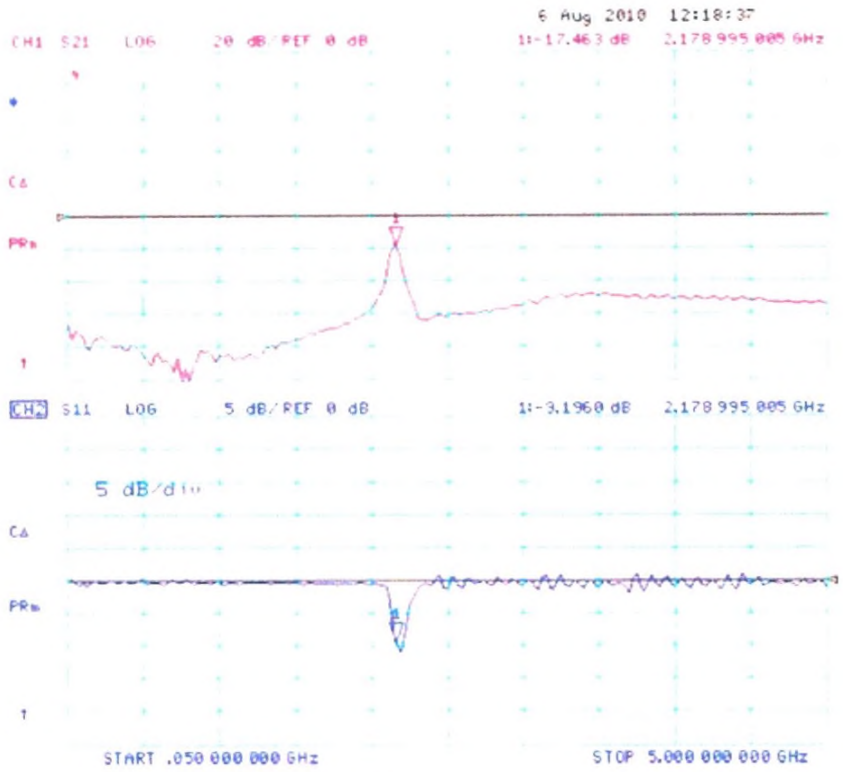


Figure 3.v.A6: Network analyzer screen dump illustrating the measured filter response.

3.v.A.1.5 Performance of the edge coupled bandpass filter.

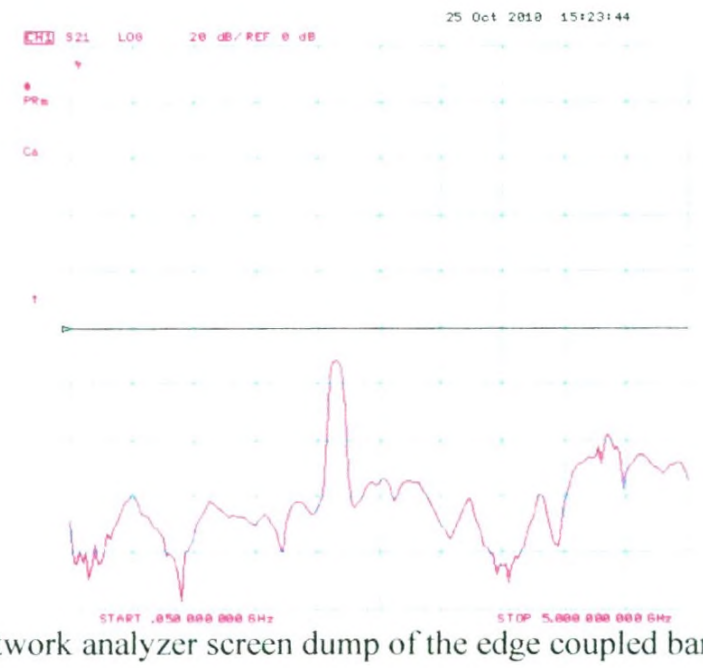


Figure 3.v.A6B: Network analyzer screen dump of the edge coupled bandpass filter.

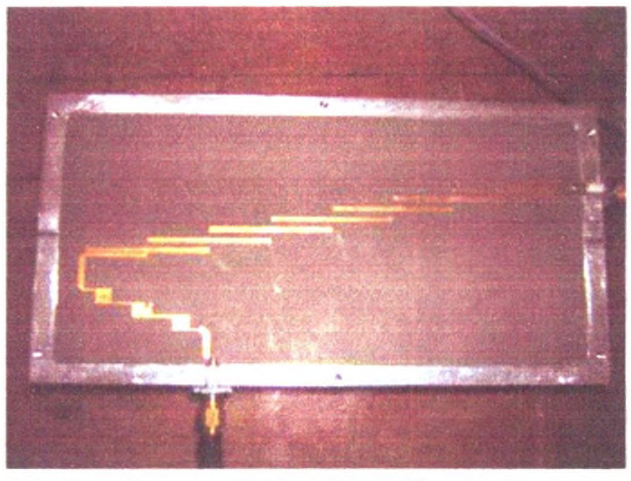


Figure 3.v.A6C: The edge coupled bandpass filter and low-pass filter cascade.

3.v.A.2 Performance measurement of stage 2

The fabricated circuit of stage 2 is shown in Figure 3.iv.A8. Initially, we faced difficulties in fabricating this circuit as HELA-10 amplifier used required heat transfer through 18 copper filled vias to the ground plane and the aluminum or brass housing. As there are no facilities to make filled vias in Sri Lanka, we tried by making a slot in the PCB underneath the device and fill it with lead.

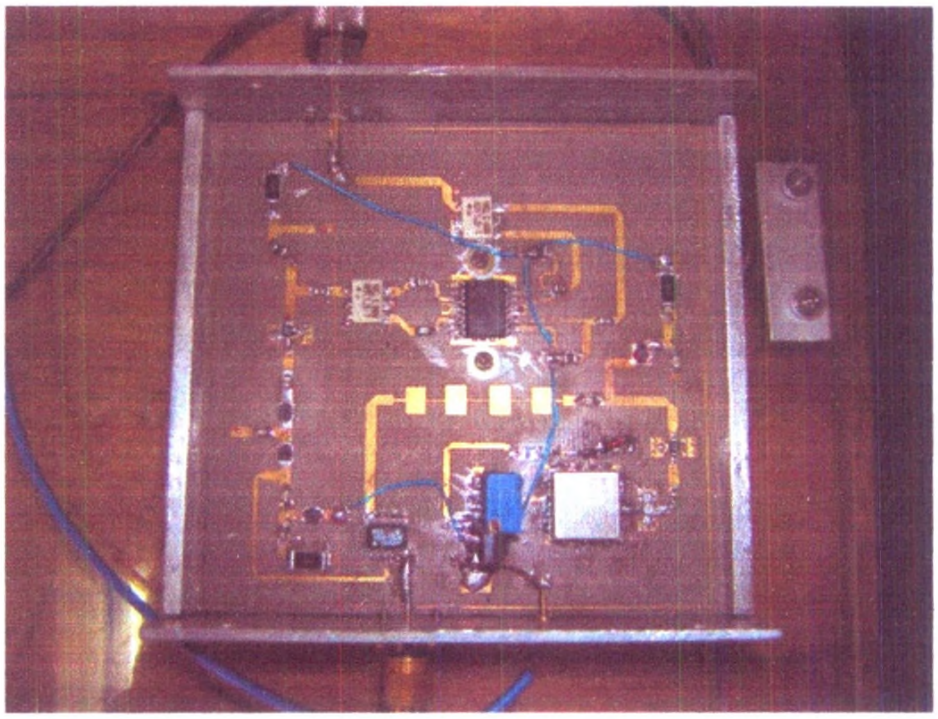


Figure 3.v.A7: Completed circuit assembly of stage 2

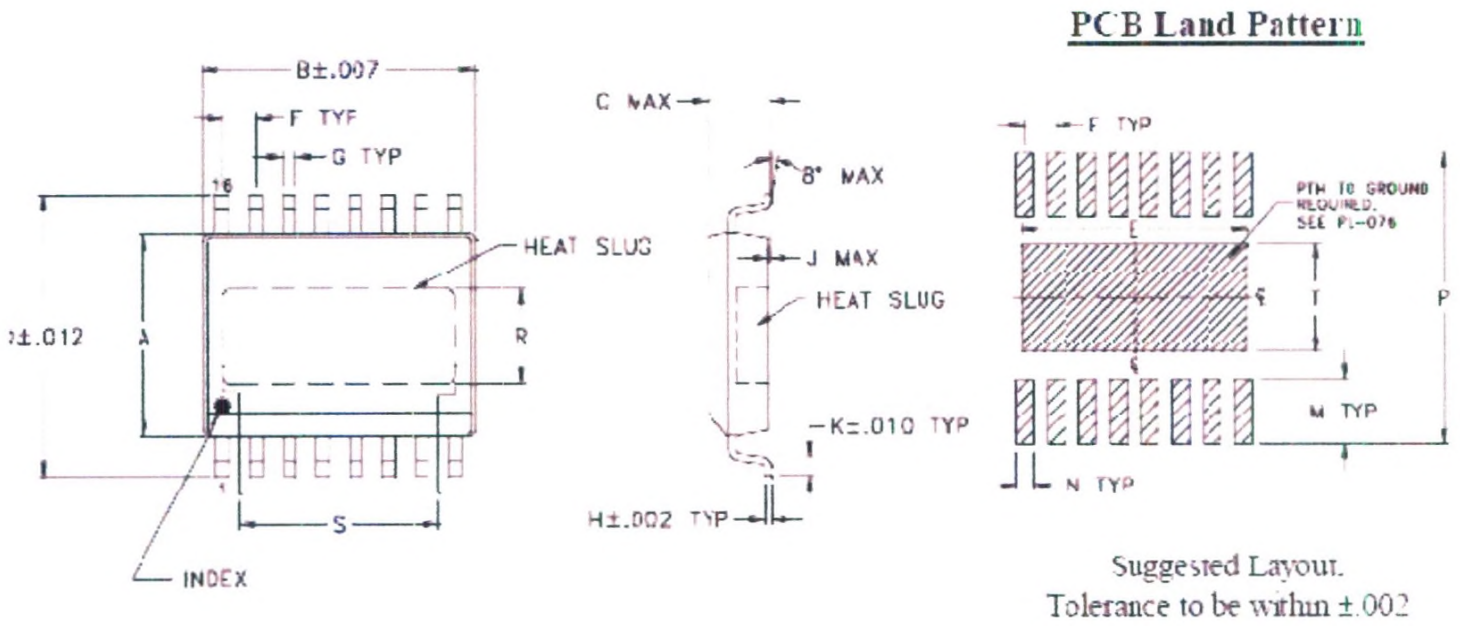


Figure 3.v.A8: Hela10D mounting instructions specified by the manufacturer

3.vA.2.1 Conversion gain measurement of stage 2

The equipment setup is similar to what we used for measuring the conversion gain of stage 1(see Section 3.v.A4.1) with one exception. We do not use the Kenwood SG7130 signal synthesizer as it can only generate signals up to 1.3 GHz. For this measurement, we need a 2.3 GHz sinusoidal signal of known power. This, we generated using stage 1 of this project. The input to stage 1 was set to -50 dBm at 800 MHz. Within stage 1, this signal was up-converted to 2.3 GHz and the power level was measured (using a spectrum analyzer) to be -44 dBm. This resulted in a power level of -30 dBm at the output of stage 2 indicating a gain of 14 dB. The gain of the second stage is expected to be 6.8 dB from simulations. However, the extra gain should not be a surprise as the circuit we fabricated does not include the insertions loss of the second I.F. filter (63 MHz SAW filter). The SAW filter is incorporated to stage 3 for ease of fabrication. [5]

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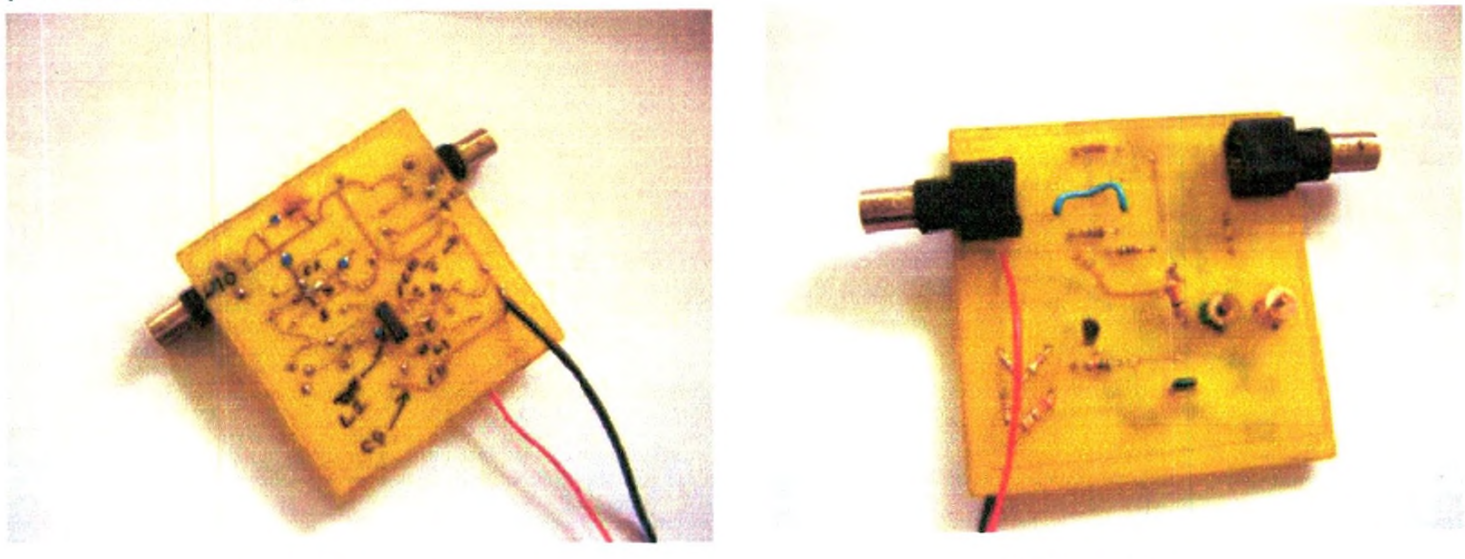
[5] Stage 2 employs ground plane technology and therefore use only surface mount components. Stage 3 is an ordinary double sided PCB which can be used to mount both through-hole and SMD components.

3.v.A.3 Performance measurement of stage 3

Figure 3.v.A9 shows the fabricated circuit of stage 3 comprising the 64 MHz crystal oscillator and the dual gate mixer. The RF input and the I.F. output are obtained via BNC connectors instead of SMA connectors as we now operate at low RF frequencies.



(a) Bottom side (b) Top side

Figure 3.v.A9: Circuits fabricated for stage 3

An alternative circuit was also fabricated with a mixer chip from Minicircuits and the SAW filter included. This is shown below.

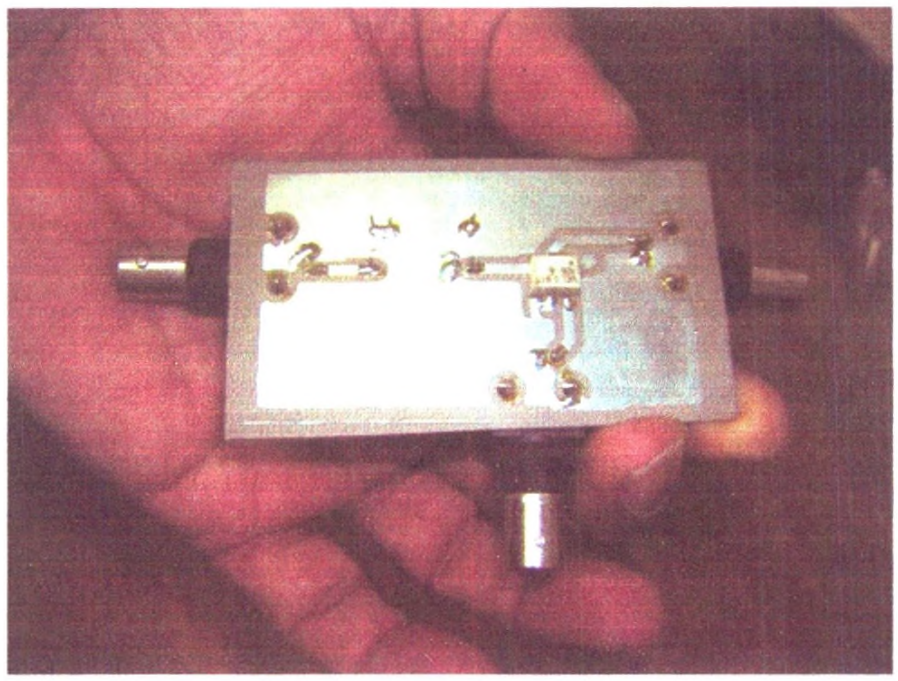
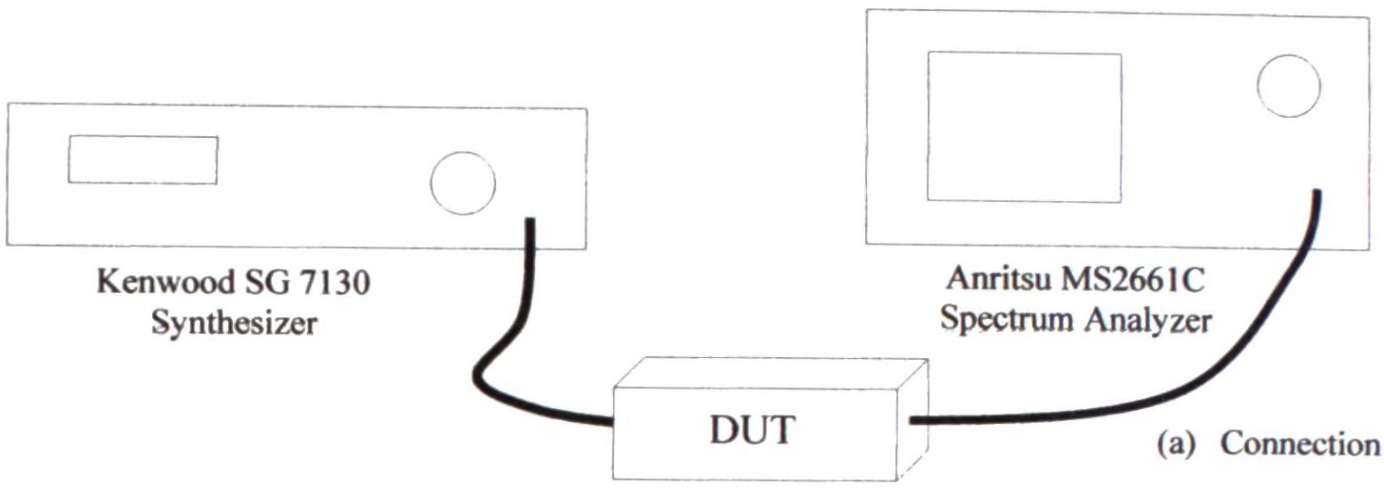


Figure 3.v.A10: Alternative third stage after tin plating

3.v.A.4 Experimental setups used for measurements

3.v.A.4.1 Experimental setup for measuring the conversion gain

The important thing about measuring the conversion gain is that the input and output are at different frequencies. The most accurate way to measure the conversion gain is by using a vector network analyzer with offset frequency measurement option. Although the DEEE of UP has a good network analyzer, it does not have the offset frequency measurement capability. Therefore, as an alternative, we use the experimental set up shown in Figure 3.v.A10. In this set up a signal of known frequency and power level is generated using a signal synthesizer is used as the input. The output power is measured using a spectrum analyzer. The spectrum analyzer is used in the carrier power measurement mode. The two power ratio was them calculated to obtain the conversion gain.



(a) Connection of equipment

(b) The actual setup

Figure 3.v.A10: Experimental set up for measuring the conversion gain.

3.viii.A References:

1. Kai Chang, "RF and Microwave Wireless Systems", John Wiley and Sons, 2000.
2. Cotter W. Sayre, "Complete Wireless Design", McGraw-Hill, 2001.
3. Agilent Application Note No 150, "Spectrum Analysis Basics".
4. MiniCircuits Application Note, "How to select a mixer".
5. Guillermo Gonzalez, "Microwave Transistor Amplifiers", Prentice Hall, 1997.
6. M. Dishal, "Alignment and adjustment of synchronously tuned multiple-resonant-circuit filters", Proc. IRE, vol. 39, pp 1448-1455, Nov. 1951.
7. S. Wong, "Microstrip tapped-line filter design", IEEE Transactions on Microwave Theory and Techniques, vol. MTT-27, pp 44-50, Jan. 1979.
8. Daniel G. Swanson, Jr., "Narrow-and microwave filter design", IEEE Microwave Magazine, vol. 8, number 5, 2007.
9. F. Harlen, "Microwave and radio-frequency exposure limits", IEE Proc., Vol 128, Pt A, No. 9, December 1981.

Part 2

3.iv.d Design of an antenna to measure the power density

Different applications demand different types of antennas based on frequency, bandwidth, angular coverage, polarization, gain etc. The antenna is an essential component of a power density meter and it has to be isotropic over the frequency band of operation.

The antennas are generally not isotropic. Therefore, the received power of an antenna depends on the direction of the incident wave and its polarization in addition to the antenna efficiency and VSWR at the feed point. Thus, in order to pick the actual power density of the incoming wave, the antenna has to be rotated in all possible directions which is a tedious and erroneous job.

The small circular loop antenna (radius $a < 0.03\lambda$) has the important property that the received power P_r is proportional to the square of the magnetic field perpendicular to the loop. I.e.

$$P_r \propto H_z^2 = H^2 \cos^2 \alpha \sin^2 \theta. \qquad (1)$$

(See Fig1). Therefore, the sum of received powers obtained by placing the loop in three orthogonal planes is proportional to the actual power density S_{avg} of the incoming wave (assuming plane waves) irrespective of its direction. I.e.

$$P_r^{total} \propto (H_x^2 + H_y^2 + H_z^2). \qquad (2)$$

$$\therefore P_r^{total} \propto S_{avg}. \qquad (3)$$

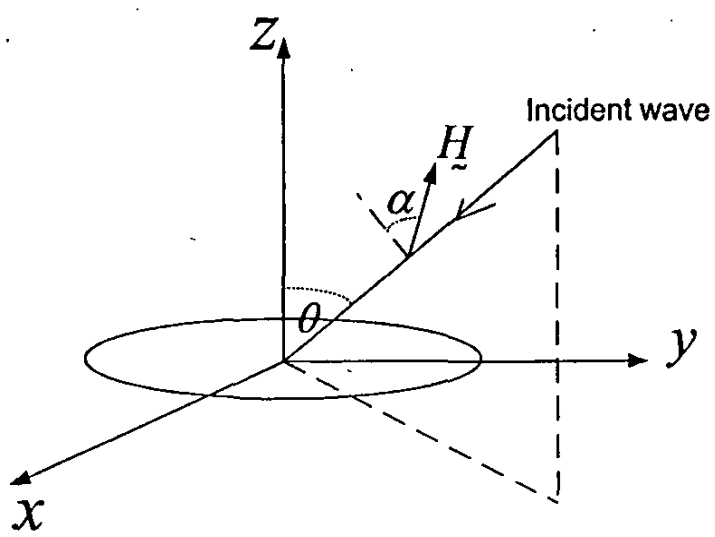


Fig. 1

In other words, three loop antennas placed orthogonally to each other forms an isotropic antenna provided loop radius $a < 0.03\lambda$. Therefore, this is the right choice of antenna for field measurements. As the first step, one loop antenna will be constructed and the incident signal power density is calculated using the power measurements obtained by placing the loop in three orthogonal planes.

By calibrating the meter the incident power density can be calculated. Theoretically, the proportionality constant can be shown to be

$$k = \frac{3\lambda^2}{8\pi} \frac{R_r}{R_r + R_l} (1 - |\rho_r|^2) \qquad (4)$$

where λ is the wave length, R_r is the radiation resistance, R_l is the loss resistance and ρ_r is the reflection coefficient at the feed point. For a small loop, all these parameters can be explicitly calculated.

For the frequency range of operation 300-1300 MHz, the required loop radius is 0.6 cm. The standard method to construct the loop antenna is to integrate the balun into the loop itself as shown in Figure 2. The loop can be made of a bare-copper semi-rigid coaxial cable with a suitable diameter, for example 0.047 mils, which is commercially available. (eg:- PE-047SR).

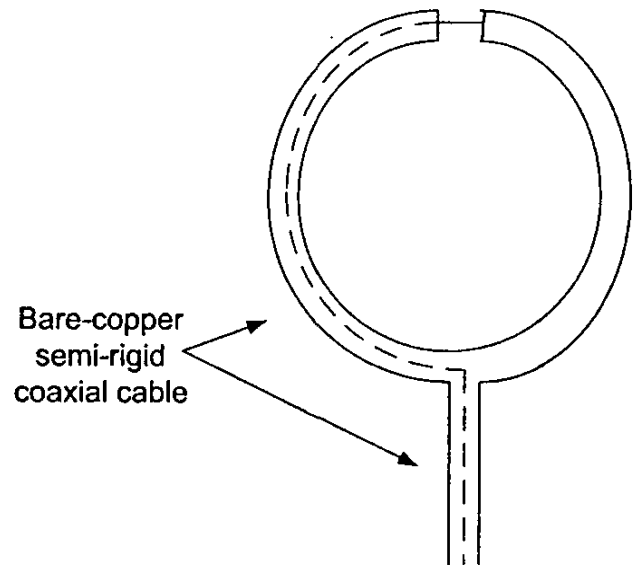


Fig. 2 Loop antenna

3.v.d Results/outputs

3.v.d.1 Characteristics of the antenna: Analytical and simulation results

Loop antenna characteristics are obtained both analytically and from simulations. The simulations results are obtained by using the commercially available electromagnetic solver HFSS (High Frequency Structure Simulator). Fig. 3 shows the characteristics of the loop. Fig. 4(a) shows the variation of the inverse of the proportionality constant ($1/k$) with frequency. The corresponding power density component (one of the three components) can be calculated from Figure 4(a) as given below.

$$S_{avg}^{x/y/z} = P_r.(\frac{1}{k}). \qquad (5)$$

The receiver is designed so that minimum power level at the receiver input is 110 dBm. Therefore the minimum detectable power density of the meter can be calculated from Fig. 4(a) and it is plotted in Fig. 4(b). These power density values are well below the practical values of typical transmitters. Eg.: power density of the field created by a mobile phone radiating 2 W of power at a distance of 1 km is 159 nW/m2.

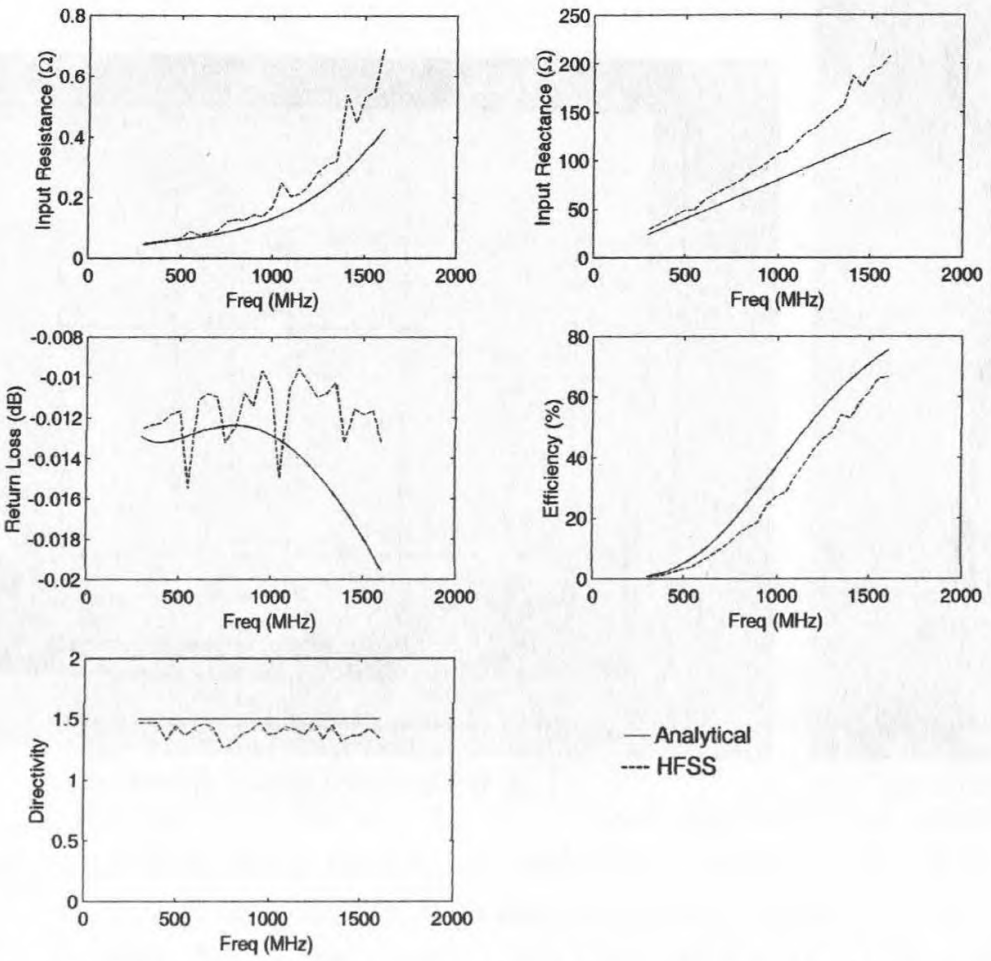


Fig. 3. Variation of typical parameters of the designed loop antenna with frequency.

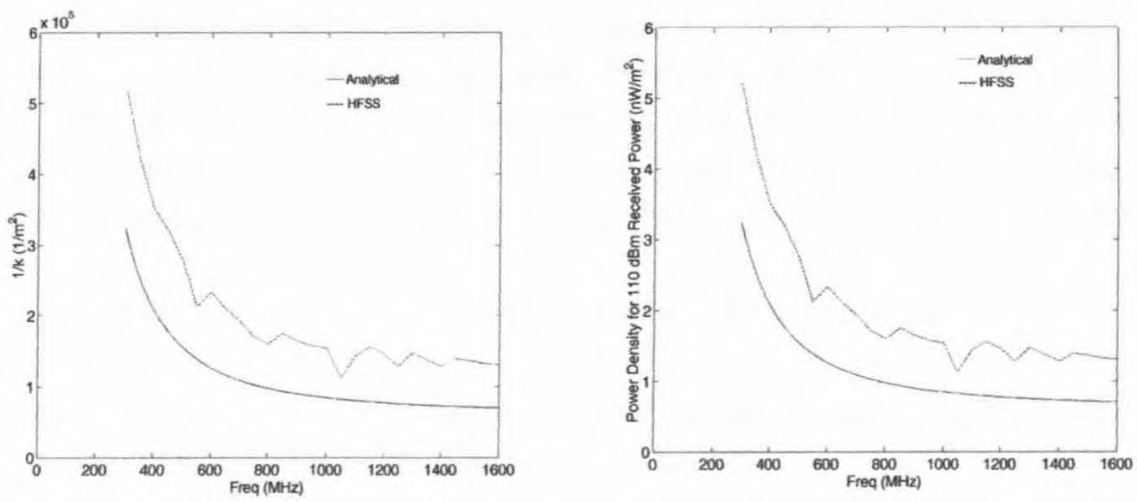


Fig. 4. (a) Variation of $1/k$ with frequency. (b) Variation of sensitivity with frequency.

3.v.d.2 Characteristics of the antenna: Measurements.

Fig. 5 shows a photograph of the constructed loop antenna and Fig. 6 shows the received signal power of the antenna measured using a spectrum analyzer over the frequency range 300-800 MHz. The antenna picked the signals around when there is no specific signal generator close by. It is clear from the Fig. 6 that the received signals are around 10db above the noise level.

Fig. 5 Constructed loop

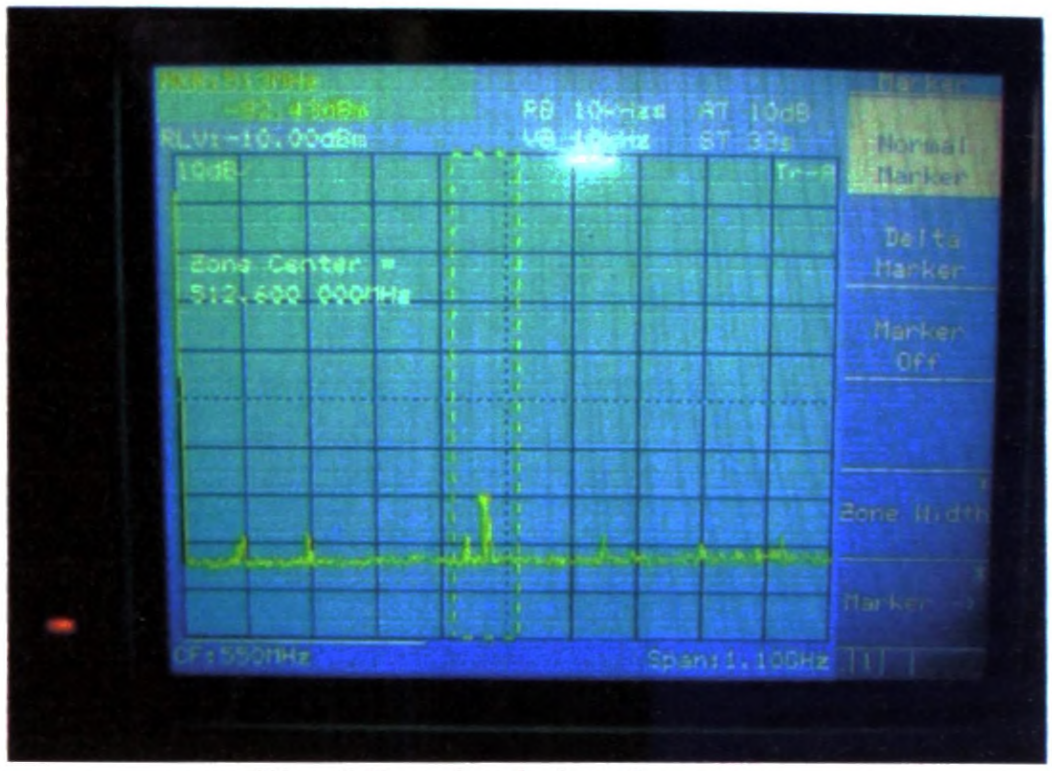


Fig. 6 Received signal spectrum

Part 3

3.iv.j IF Energy/Power Measurement and Display

3.iv.j1 Introduction

This section describes the design and construction of the signal acquisition and display module, 5MHz digital clock, frequency auto scanner, high gain 1MHz amplifier and the regulated power supply unit. It also discusses the reasons for selecting the particular IF frequency and the sampling rate and then the two main integrated circuits PIC18F4550 and Maxim 1426 ADC.

3.iv.j1.1 Frequency Conversion

The UHF signal must be down converted to a convenient working frequency (f_w) for energy and power estimation. A frequency of 1MHz was selected for this purpose for two main reasons. The first is that if the signal is to be processed in a computer, A/D conversion is necessary. Therefore, f_w should be low enough so that sample acquisition will be possible using a circuit based on an available USB microcontroller, i.e. PIC18F4550, [2]. If the sampling rate is in the order of 1MS/s, the design and fabrication of acquisition circuits already pose significant challenges making it costly and complex. Secondly, the working frequency should be as high as possible such that wideband signals can be measured. The selected 1MHz frequency has a maximum signal bandwidth of 2MHz which makes it possible to evaluate all 2G mobile signals and 1.25MHz 3G MC-CDMA signals.

In this way, the energy and power can be evaluated by mathematical processing of sample values after acquiring them into the computer. However, it is also possible to process the 1MHz signal using analog circuits. For example, an analog integrator would accumulate the energy over a certain time window and then display the result in a moving coil instrument. Alternatively, a peak detector circuit would display the signal level on an oscilloscope.

The following parameters were essentially considered in the design of energy and power estimation units.

i) Minimum sampling rate for the purpose of power measurement: As described in section 3.iv.j1.3, for a sinusoid, this is at least four times the frequency.

ii) Signal bandwidth: This determines the sampling rate and the A/D converter specifications. For example, for a signal with 200kHz bandwidth, the sampling rate must be greater than 4.4 MS/s, i.e. (1MHz + 200kHz/2)×4.

iii) Dynamic range, the number of bits per sample and the bit rate: To cover a 2.56v dynamic range with a 10mv accuracy 8bits/sample is required ($2.56v/2^8$levels= 10mv), which sets a data rate of 35.2Mbps (4.4MS/s×8). The MAXIM 1426, [3] A/D convertor, for example, meets this specification which has a resolution of up to 10 bits/sample and a maximum sampling rate of 10Ms/s.

iv) Interfacing hardware for the computer: The USB interface of the PIC18F4550 microcontroller supports a maximum data rate of 12Mbps. Therefore, this necessitates using some form of delta modulation to reduce the original bit rate for real time streaming of data. Otherwise, store and forward interfacing where some signal samples are stored in the microcontroller and fed to the computer at a lower rate, can be used for this purpose. However, the signal can be observed only intermittently with this approach.

3.iv.j1.2 Power and Energy Estimation

In general, the average power of a signal could be estimated by squaring the signal voltage and integrating it over a suitable time duration as follows.

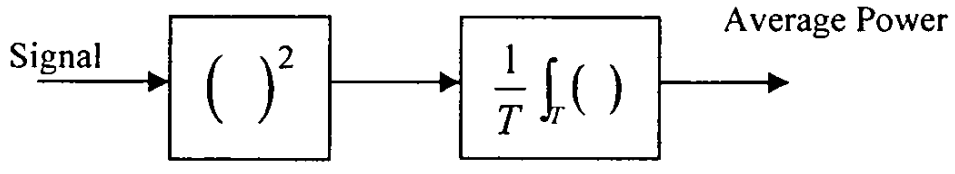


Fig. 1: Power estimation of a signal

The reliability of the estimates would vary depending on the type of the signal processing used, for example, the analog signal processing and the digital signal processing. These two methods could be simply illustrated with the following block diagrams.

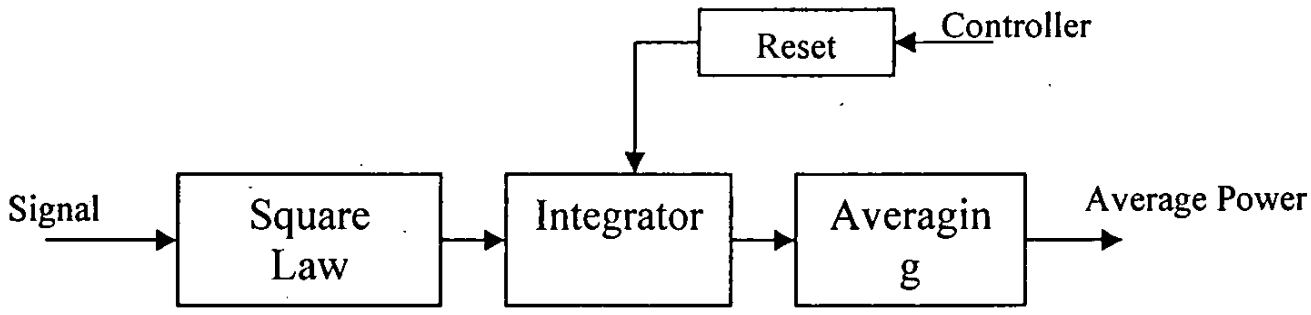


Fig. 2: Power estimation using analog signal processing

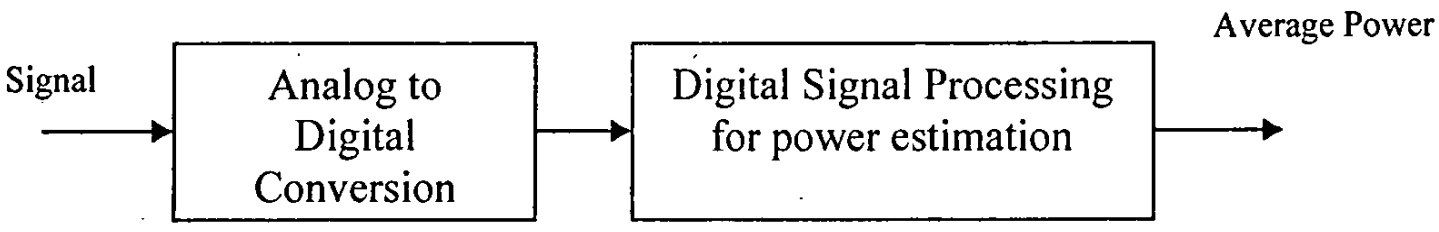


Fig. 3: Power estimation using digital signal processing

Power or energy estimation using analog signal processing can be implemented in hardware using lumped components such as BJTs, diodes, capacitors, resistors and as a result the circuit is less flexible and the estimates are less accurate. However, with digital signal processing, it is easy to manipulate signal samples, providing more flexibility. The samples could be digitized and read into a DSP, a microcontroller or a computer to estimate the power and energy in a required band width.

3.iv.j1.3 Signal Bandwidth and Sampling Rate

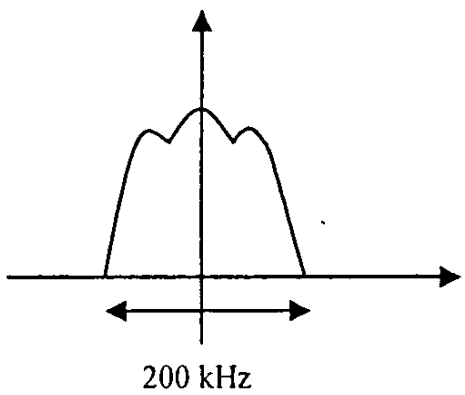


Fig. 4: Spectra of the signal

Say, the total bandwidth of the UHF signal is 200 kHz. Once down converted to an intermediate frequency of f_w=1MHz, the maximum frequency component in the signal is 1 MHz + 100 kHz = 1.1 MHz.

Therefore, the minimum sampling rate required (Nyquist sampling) = 2x1.1 MHz
= 2.2 MHz

However, for the purpose of power and energy measurement, a higher rate is required as described here.

Consider a sinusoidal waveform; $A_c \text{Cos } \omega_c t$

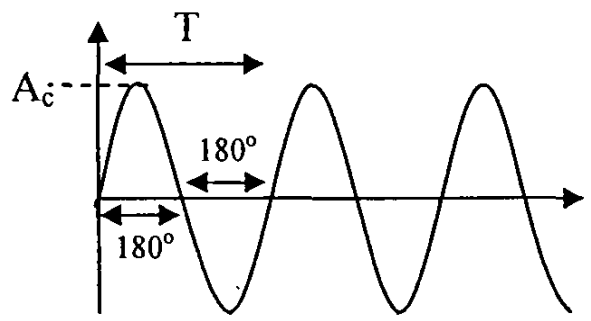


Fig. 5: Sinusoidal waveform

The average power of the above signal = $A_c^2/2$ because

$$\frac{1}{T}\int_0^T A_c^2 \cos^2\omega_c t.dt = \frac{1}{T}A_c^2 \int_0^T \frac{1}{2}[1+\cos 2\omega_c t].dt$$

$$= \frac{A_c^2}{2T} \times T$$

$$= \frac{A_c^2}{2}$$

1. If this signal is sampled at the Nyquist rate; (2 times the maximum frequency)

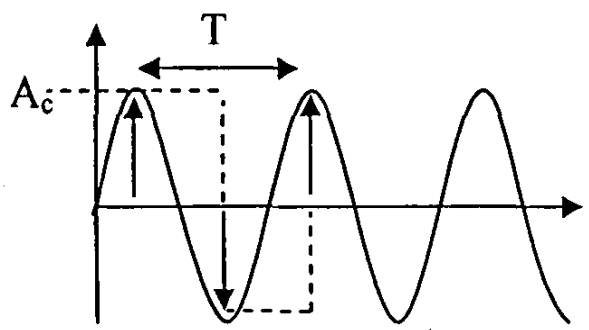


Fig. 6: Sampling at 2 samples/cycle

$$\text{The average power} = \frac{1}{T}\left\{\frac{T}{2}A_c^2 + \frac{T}{2}A_c^2\right\} = A_c^2$$

$$\text{The error} = A_c^2 - \frac{A_c^2}{2} = \frac{A_c^2}{2}$$

Therefore, this sampling rate gives an error of 100% for power and energy estimation.

2. Sampled at twice the Nyquist rate; (4 times the maximum frequency)

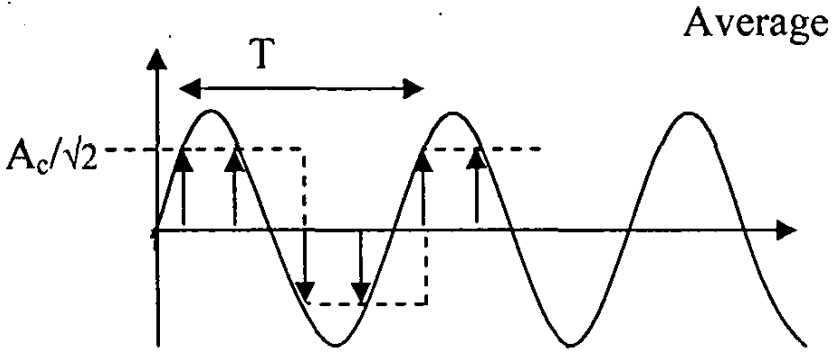


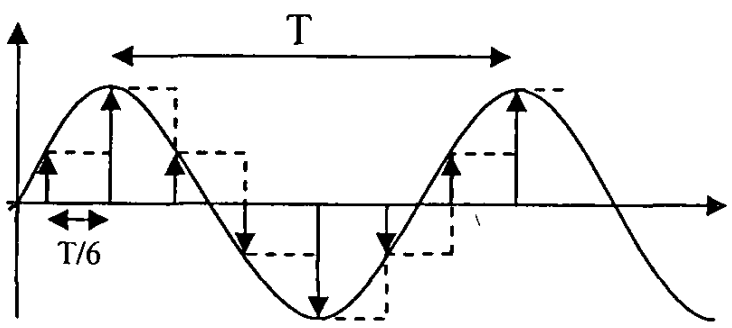
Fig. 7: Sampling at 4 samples/cycle

$$\text{Average power} = \frac{1}{T}\left\{\frac{T}{2}\left(\frac{A_c}{\sqrt{2}}\right)^2 + \frac{T}{2}\left(\frac{A_c}{\sqrt{2}}\right)^2\right\} = \frac{A_c^2}{2}$$

$$\text{The error} = \frac{A_c^2}{2} - \frac{A_c^2}{2} = 0$$

Therefore, a sampling rate of 4 times the maximum frequency provides a correct power and energy estimate for sinusoidal signals.

3. Sampled at three times the Nyquist rate; (6 times the maximum frequency)



Sample values per cycle;

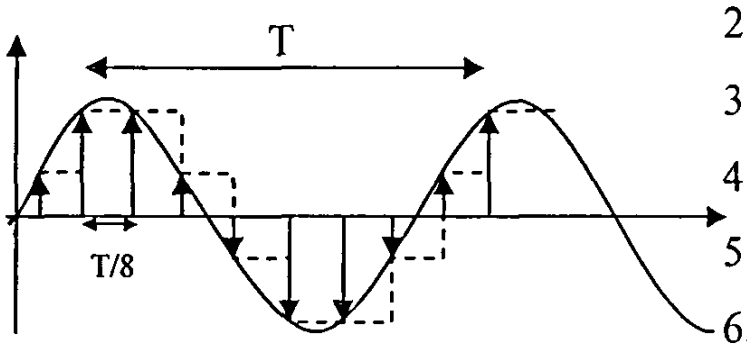
1. $A_c \sin 30^o = 0.5A_c$
2. $A_c \sin 90^o = A_c$
3. $A_c \sin 150^o = 0.5A_c$
4. $A_c \sin 210^o = -0.5A_c$
5. $A_c \sin 270^o = -A_c$
6. $A_c \sin 330^o = -0.5A_c$

Fig. 8: Sampling at 6 samples/cycle

$$\text{Average Power} = 2 \times \frac{1}{T}\left\{\left(\frac{A_c}{2}\right)^2 \frac{T}{6} + \left(A_c\right)^2 \frac{T}{6} + \left(\frac{A_c}{2}\right)^2 \frac{T}{6}\right\} = \frac{A_c^2}{2}$$

$$\text{The error} = \frac{A_c^2}{2} - \frac{A_c^2}{2} = 0$$

4. Sampled at four times the Nyquist rate ;(8 times the maximum frequency)



Sample values per cycle;

1. $A_c \sin 22.5^o = 0.38268A_c$
2. $A_c \sin 67.5^o = 0.92387A_c$
3. $A_c \sin 112.5^o = 0.92387A_c$
4. $A_c \sin 157.5^o = 0.38268A_c$
5. $A_c \sin 202.5^o = -0.38268A_c$
6. $A_c \sin 247.5^o = -0.92387A_c$
7. $A_c \sin 292.5^o = -0.92387A_c$
8. $A_c \sin 337.5^o = -0.38268A_c$

Fig. 9: Sampling at 8 samples/cycle

$$\text{The Average power} = 4 \times \frac{1}{T}\left\{\left(0.38268A_c\right)^2 \frac{T}{8} + \left(0.92387A_c\right)^2 \frac{T}{8}\right\} = \frac{A_c^2}{2}$$

$$\text{The error} = \frac{A_c^2}{2} - \frac{A_c^2}{2} = 0$$

Therefore, for a sinusoid, a sampling rate which is four times the maximum frequency would give an accurate power estimation.

For example;
In GSM, GMSK is used for smooth transition from one frequency to other. Most of the power (90%) in GMSK modulation is within the 200 kHz bandwidth.

Therefore, at a working frequency of 1 MHz, the maximum frequency GMSK signal could have is; f_{max}= 1MHz+ (200/2) kHz = 1.1MHz.
Therefore, the suitable sampling frequency must be $\geq 4 \times 1.1 = 4.4$ MHz.

3.iv.j1.4 Sample Acquisition

If we use a sampling frequency of 10 MHz, which is well above the minimum of 4.4MHz, then with a resolution of 8 bits/sample, 10x 8 = 80Mbits will be generated per second.

Therefore, the interface should operate at 80 Mbps in order to read the samples into the PC. If a serial communication link is to be used as the interface, it should have a throughput capacity of 80 Mbps. However, this is only possible with high speed USB or Fast Ethernet. In addition, the PC should be able to handle such a high rate of data flow.

With the first option, the practical implementation of Fast Ethernet/High Speed USB requires an FPGA platform. Due to the high cost of FPGA's, a cheaper option has to be chosen.

The interfacing unit should receive the bit stream from the A/D convertor and then forward it to the PC as illustrated in the fig 10.

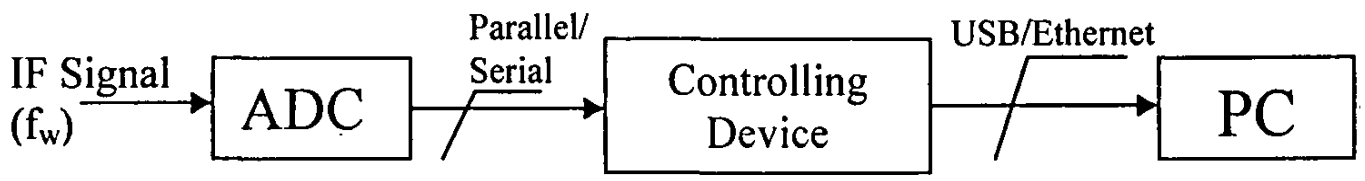


Fig 10: Interfacing ADC and PC

The data rate of the interface is a critical factor in determining the interfacing unit. The possible interfacing methods could use full speed USB (12 Mbps) or Ethernet (10Mbps). However, with these devices, it is not possible to process an 80 Mbps bit stream. Therefore, it is necessary to reduce the rate below 12 Mbps by using an encoding scheme. Considering the sampling rate of 10 MS/s, the possible approach is to use delta modulation [4, 5], where one bit is generated for each sample. This scheme theoretically results in a rate of 10 Mbps enabling the A/D converted bits to be sent serially to the computer/processing unit. Considering the overhead bits needed for interfacing/communication with the computer, the Ethernet (10 Mbps) option has to be dropped and the only choice available is the full speed USB with 12 Mbps data rate.

A major challenge would be to reduce the addition of overheads to keep the throughput below 12 Mbps. Therefore, a USB controller which could monitor both the ADC and the USB interfacing is needed to ensure the smooth operation. For this purpose, a microcontroller with a USB port and a USB controller such as the PIC18F4550 manufactured by Microchip provides a reasonable hardware support. It consists of a full speed (12 Mbps) USB 2.0 controller and a USB port and is capable of processing at 12MIPS with a 48MHz clock.

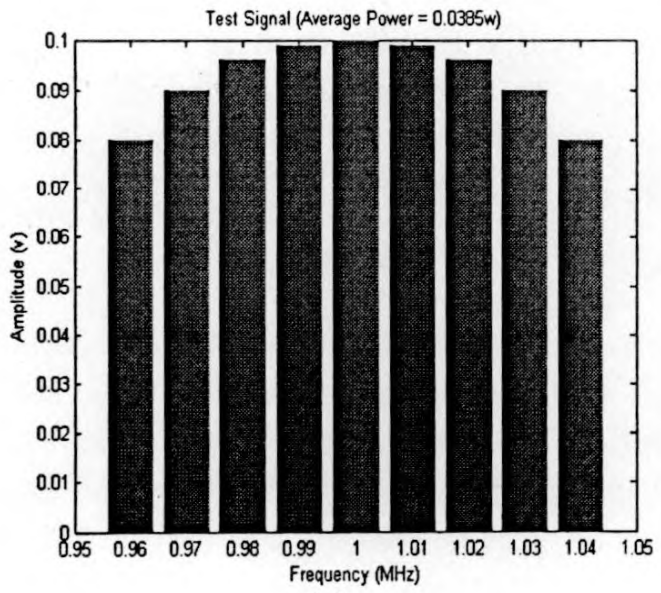
3.iv.j1.5 Delta Modulation with Fractional Differences (DMFD)

The disadvantage with the original 1-bit delta modulation is that the accuracy of signal estimation decreases rapidly with the presence of frequencies other than the purely 1MHz centre frequency. In addition, a reference signal sample (in the form of an 8-bit word) has to be sent regularly. Otherwise, the demodulator fails to track the signal after a few milliseconds.

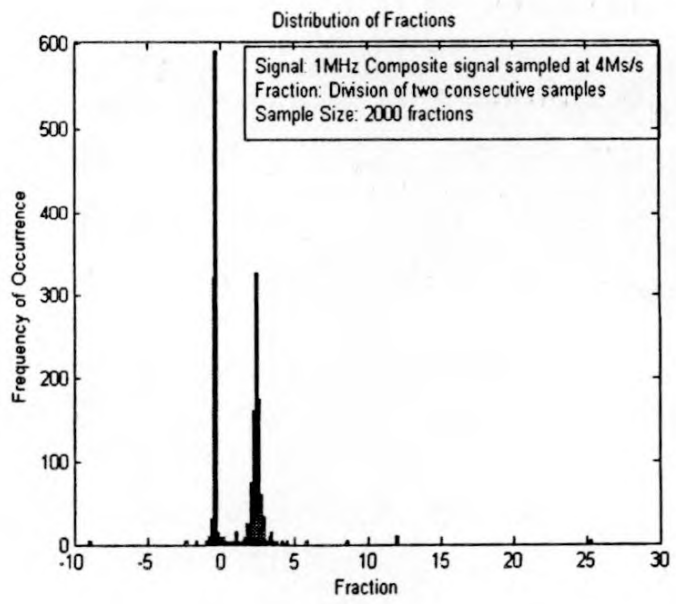
An approach to improve delta modulation/demodulation is to increase the number of bits/sample which carries the fractional differences of the previous and current samples rather than the sign of the increase in normal delta modulation. Once this is implemented with the PIC18F4550, the sampling rate of the A/D converter has to be decreased to 4MHz such that 3 bits can be allocated per sample utilizing the maximum USB rate of 12Mbps. This adds some inaccuracy to the energy estimation because minimum sampling rate should be 4.4MHz as indicated previously to cover a bandwidth of 200kHz. In addition, the PIC processor must divide two samples and do 3 bit binary encoding (BCD). If there are more than 8 different fractions, they must be rounded off to the nearest most common fraction such that the total is eight. This scheme works perfect for a single frequency as the number of different fractions is always 2 when sampled at 4 times. However, the presence of other frequencies even over a bandwidth of 200kHz can yield more fractions than 8. This increases the inaccuracy further when fractional differences are demodulated and the energy is estimated.

For example, the composite signal illustrated in Fig.11a was formed by adding 8 nearby frequencies to the 1MHz centre frequency, over a bandwidth of 200kHz. Once this composite signal was sampled at 4MHz (90.9% under-sampling), there were a large number of different fractions as illustrated in the histogram in Fig. 11b but most of them were either very similar or occurred rarely. It is easily seen from Fig. 11c that those fractions which are very frequent compared to the rest are about eight for this test signal.

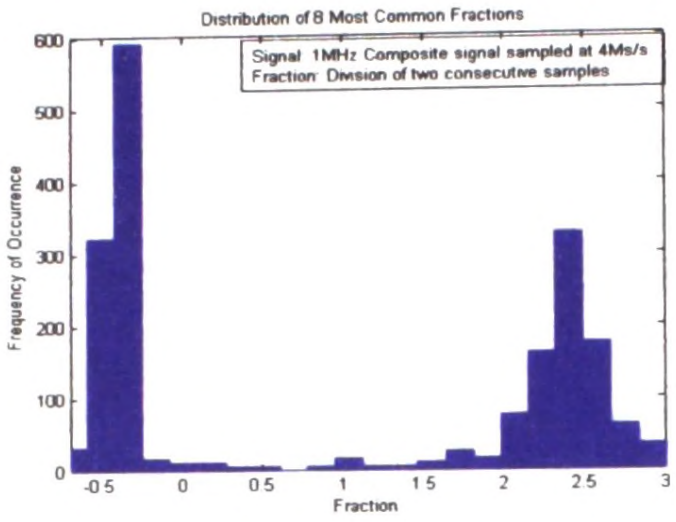
Fig. 12a illustrates the accuracy of signal reconstruction and power estimation once the signal samples are encoded and decoded using all possible fractions. If the number of possible fractions is L, encoding requires N bits per sample where $N=\text{Log}_2(L)$. The discrepancy in signal tracking and power estimation here is only due to under-sampling. However, using a set of most common 8 fractions and then 3-bit encoding per sample, a good approximation can be made to the test signal as illustrated in Fig. 12b. The discrepancy here is both due to under-sampling and limiting fractional differences.



(a)

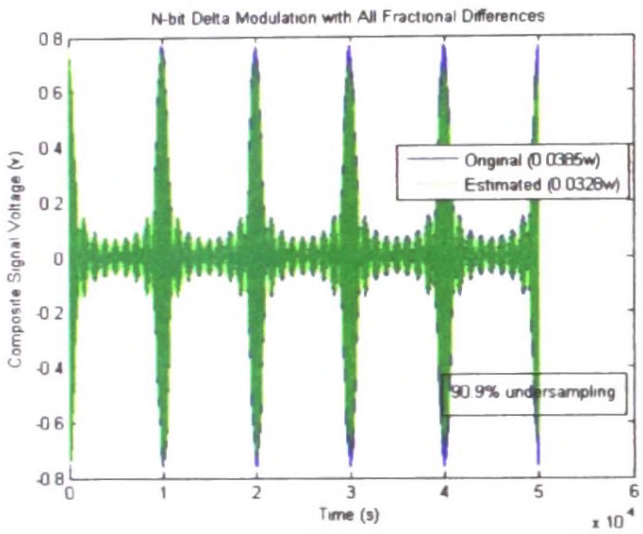


(b)

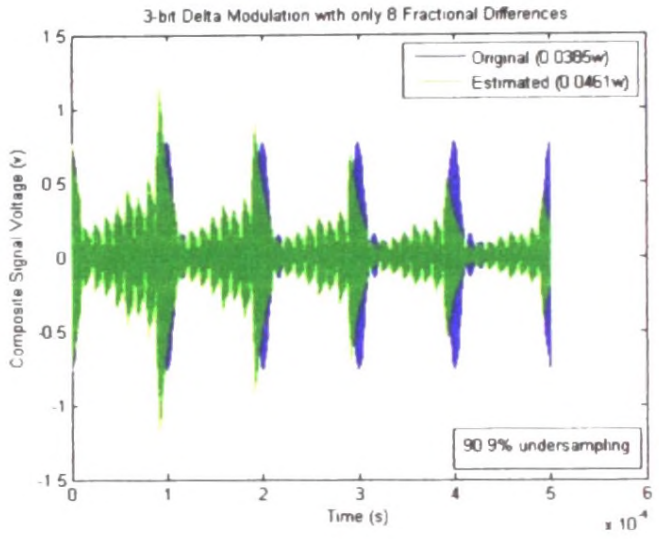


(c)

Fig. 11: Composite Test Signal and the Distribution of Fractional Differences



(a)



(b)

Fig. 12: N-bit and 3-bit Delta Modulation

For the implementation, 8-bit reference samples must be inserted into the bit stream from time to time to assist the demodulator for re-synchronization. Note that for true representation of the signal, another bit is required to convey the sign of the fraction. However, for energy estimation, the sign bit is redundant.

The illustrated example considers a signal with very rapid changes in the envelope every 0.1ms. Three-bit DMFD can reconstruct even this signal with a reasonable degree of accuracy implying that it would be very accurate for a signal with smoother fluctuations.
(Note that although the normal 1-bit delta modulation can accurately reconstruct the signal, the sampling rate has to be much higher than 4 times the maximum frequency).

3.iv.j2 Prototype Implementation with Store & Forward Interfacing

The PIC18F4550 has 2 kbytes of data memory which can be used for storing A/D converted signal samples. In this case 512 samples of the signal is stored in this memory before streaming. If the sampling rate is 5MHz, allowing a bandwidth of 500kHz centered at 1MHz, this number of samples represent about 0.1ms of the signal time. Then, the whole 2kbyte file can be streamed to the computer via the USB controller, during which time the input signal is not processed. Once the streaming is over, the signal can be sampled in again and again. The other advantage is that this method of storing and forwarding signal samples simplifies PIC programming by a great extent, utilizing the maximum speed of the PIC. This approach is not unsuitable for this project because the energy/power estimation is more accurate when random sets of samples are processed rather than a long continuous sequence. In addition, all the UHF frequencies are monitored one after the other in a round robin fashion. Therefore, continuous sampling of a given UHF frequency is not necessary anyway.

Note that although it may be possible to store a larger number of samples in the 32kbyte program memory, that approach was not taken due to the following reasons.

i) Time delay involved with storing and then forwarding data samples in the order of 10's of kbytes is excessively high.

ii) It was found that the PIC program written in PIC C for the purpose of reading in A/D converted samples and writing to the USB output, consumes about 16kbyte of the program memory. The whole 32 kbyte program memory could later be needed to extend the PIC C program for continuous streaming of data samples using Delta Modulation with Fractional Differences (DMFD), as described in the previous section.

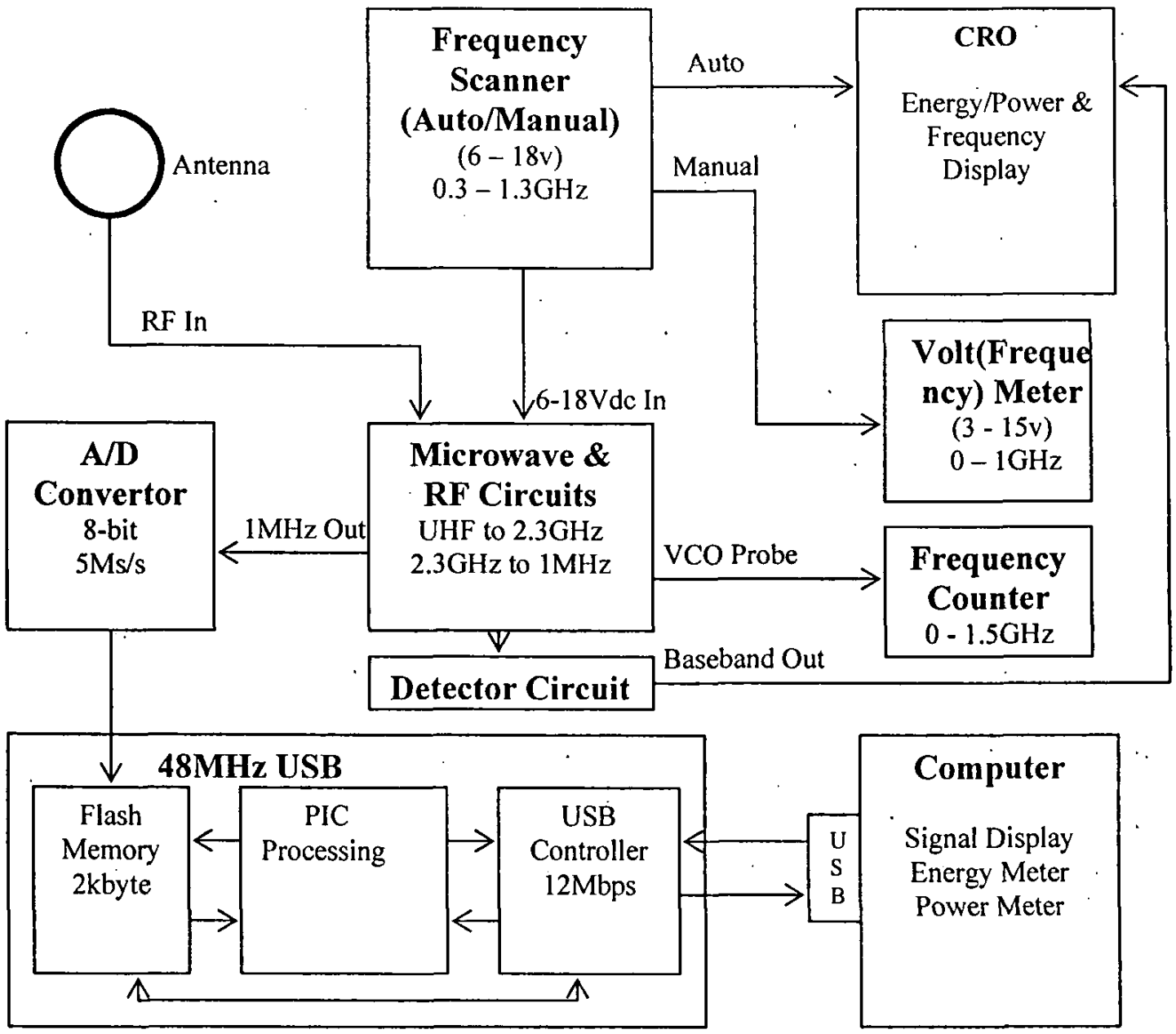


Fig. 13: Store & Forward Interfacing

As illustrated in Fig. 13, once a given set of 512 samples has been processed the computer displays the 512 signal values, the energy meter and the power meter in a real time window. The energy meter and power meter readings are calculated considering multiple sets of 512 samples, which is adjustable. The default is 100 sets which correspond to a time duration of 10ms.

The UHF input frequency can be measured using both a standard frequency counter (0 – 1.5GHz) and a calibrated voltmeter. The voltmeter reads the VCO tuning voltage of the first microwave circuit over the linear range from 3 to 15v which corresponds to a frequency range of 0 to 1GHz.

In addition, there is a CRO display which displays the received signal level against the RF frequency using the **X-Y** mode. A time base signal scans frequencies ranging from 0.3-1.0GHz up and down for this purpose.

3.iv.j2.1 Main Circuit Modules of the USB Signal Reader

1. 10MS/s, 10-bit MAXIM 1426 A/D Converter and the associated biasing circuitry.

   The MAXIM 1426 has been used to sample a ±2v input with the help of CML input. The input signal is isolated by the 50Ω transformer with almost 1:1 turns ratio. The centre tap of the secondary is connected to the CML input. The REFN is grounded to accept the CML input. The other external reference inputs REFIN and REFP are bypassed using 0.1μ capacitors. The CMLP and CMLN common mode level inputs are connected to the supply and the GND for AC coupling. The OE/PD has been used as a standby (power-down) switch by selecting either the supply or the GND through a switch.

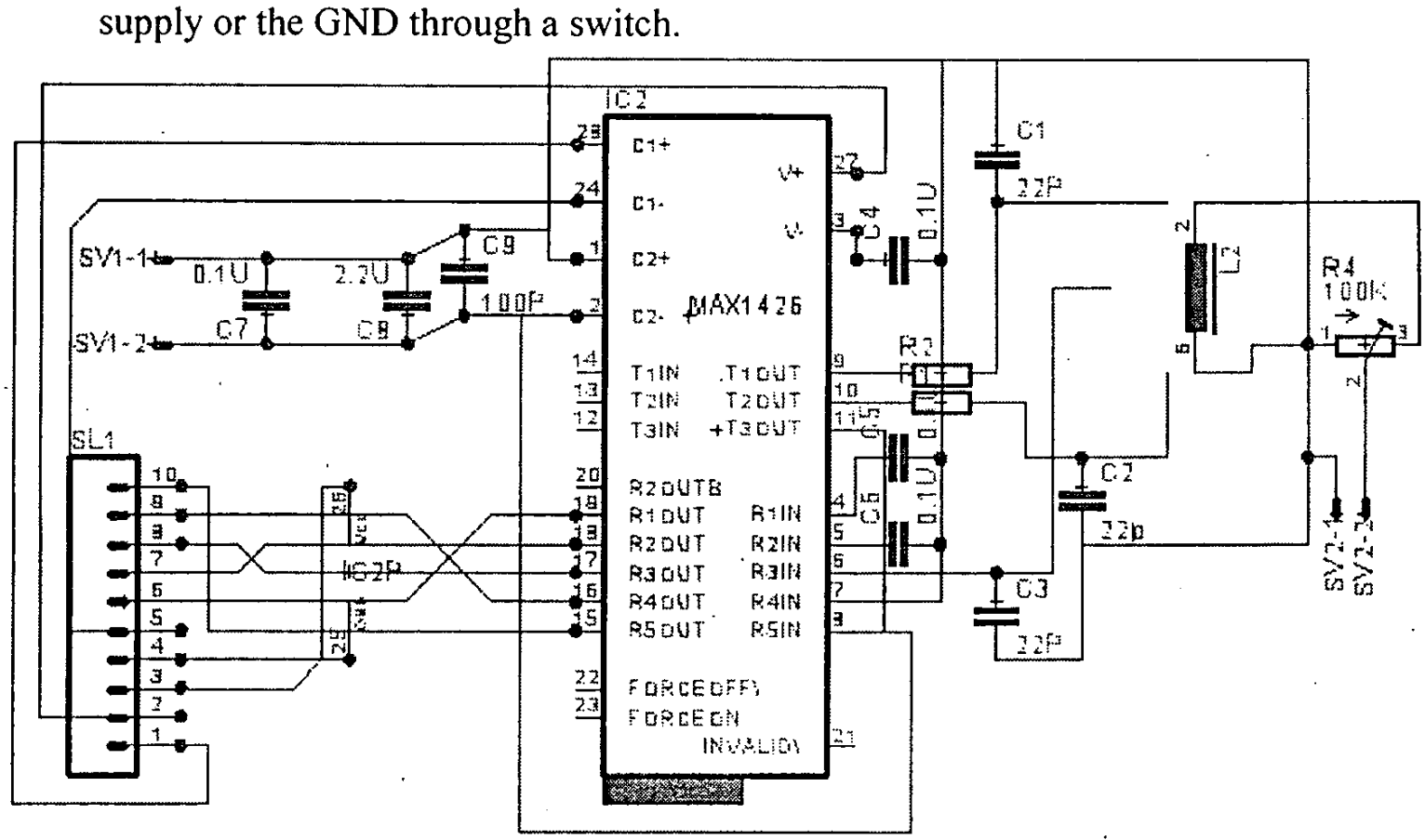


Fig. 14: 5MS/s, 8-bit A/D Converter Circuit

2. 5MHz system clock fabricated using a crystal oscillator, amplifier and logic gates.

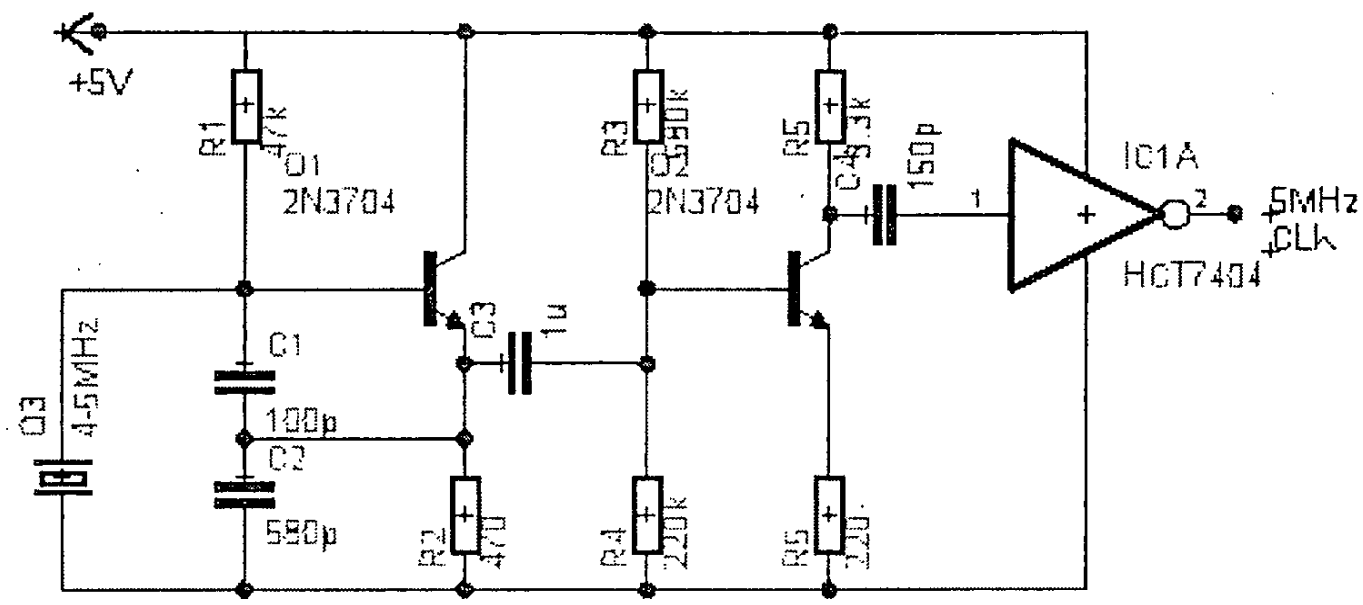


Fig. 15: 5MHz Clock Circuit

After obtaining the oscillations from the crystal circuit(Q1, Q3), the common emitter (Q2) is used to raise the signal level to drive the logic NOT gate. The logic gate provides a 5v square wave signal.

3. PIC18F4550 microcontroller and the associated biasing circuitry with a 20MHz crystal.

4. High gain amplifier tuned to 1MHz frequency.

   After down converting the UHF signal to 1MHz using several microwave and RF stages, the signal power is raised to the required level by using two common emitter stages. A very high open circuit gain close to 75dB can be obtained over a limited frequency range with this configuration. The USB reader has an input impedance of 3.5kΩ. The amplifier can still provide a gain close to 70dB for a 3.5kΩ load, without distortion for less than 1mv inputs.

   However, if the input to the amplifier exceeds 1mv, the two supply voltages must be increased such that signal distortion is avoided.

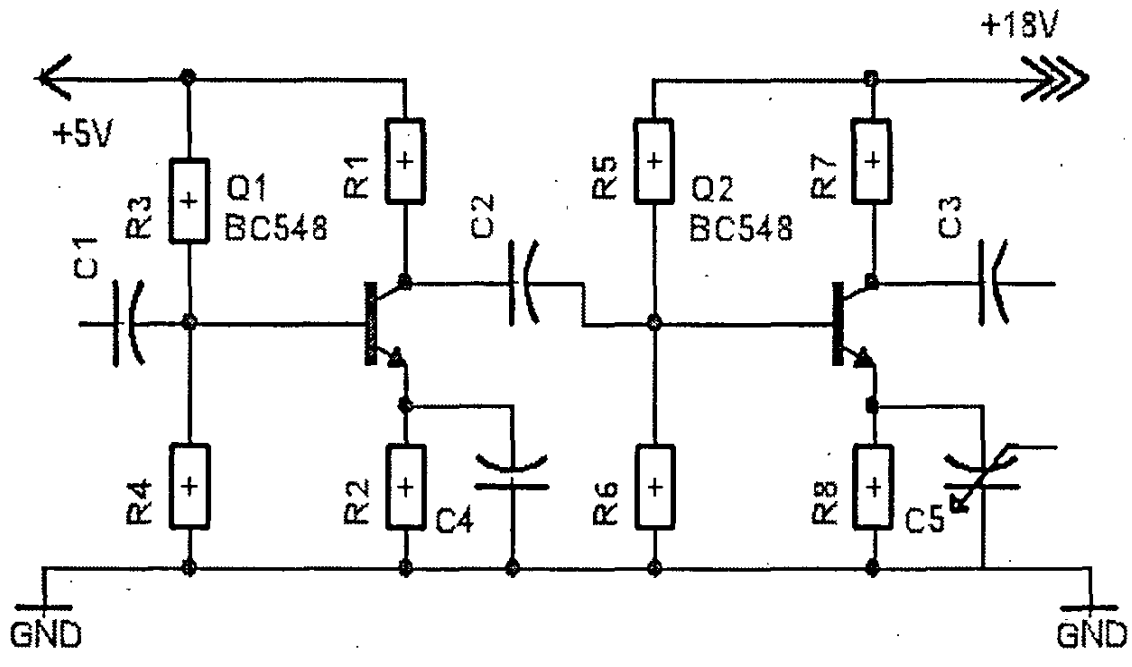


Fig. 16: 1MHz High Gain Amplifier Circuit

3.iv.j2.2 Software: Delphi project with several sub programs for computer display
Once the 512 sets of signal samples are streamed to the USB port of the computer, they are read by using a real time Delphi program. The program consists of three main modules for reading samples (Thread), maintaining a real time window (Wnd) and processing data and displaying measurements (OscopeDisplay). Once the 'Oscope' executable file is run, the display window in Fig. 17 displays the 512 signal samples in sequence.

The 'OscopeThread', 'OscopeWnd' and OscopeDisplay' has further been developed such that they calculate the signal energy and power over a certain time period and display in the same window.

The signal energy has been determined by accumulating the instantaneous power of each sample normalized to a 1 ohm resistor as $E = \sum_i \frac{v_i^2}{1}$; $i = 1,2....512 \times n$, where v_i is the sample magnitude in volts and n is the number of 512 sample sets considered for the calculation.

The signal power, P, is then the sample average of E, which is $P = \frac{E}{512 \times n}$.

An energy meter and a power meter have also been implemented inside the 'OscopeDisplay' program. They appear within the display window and display the real time energy and power readings.

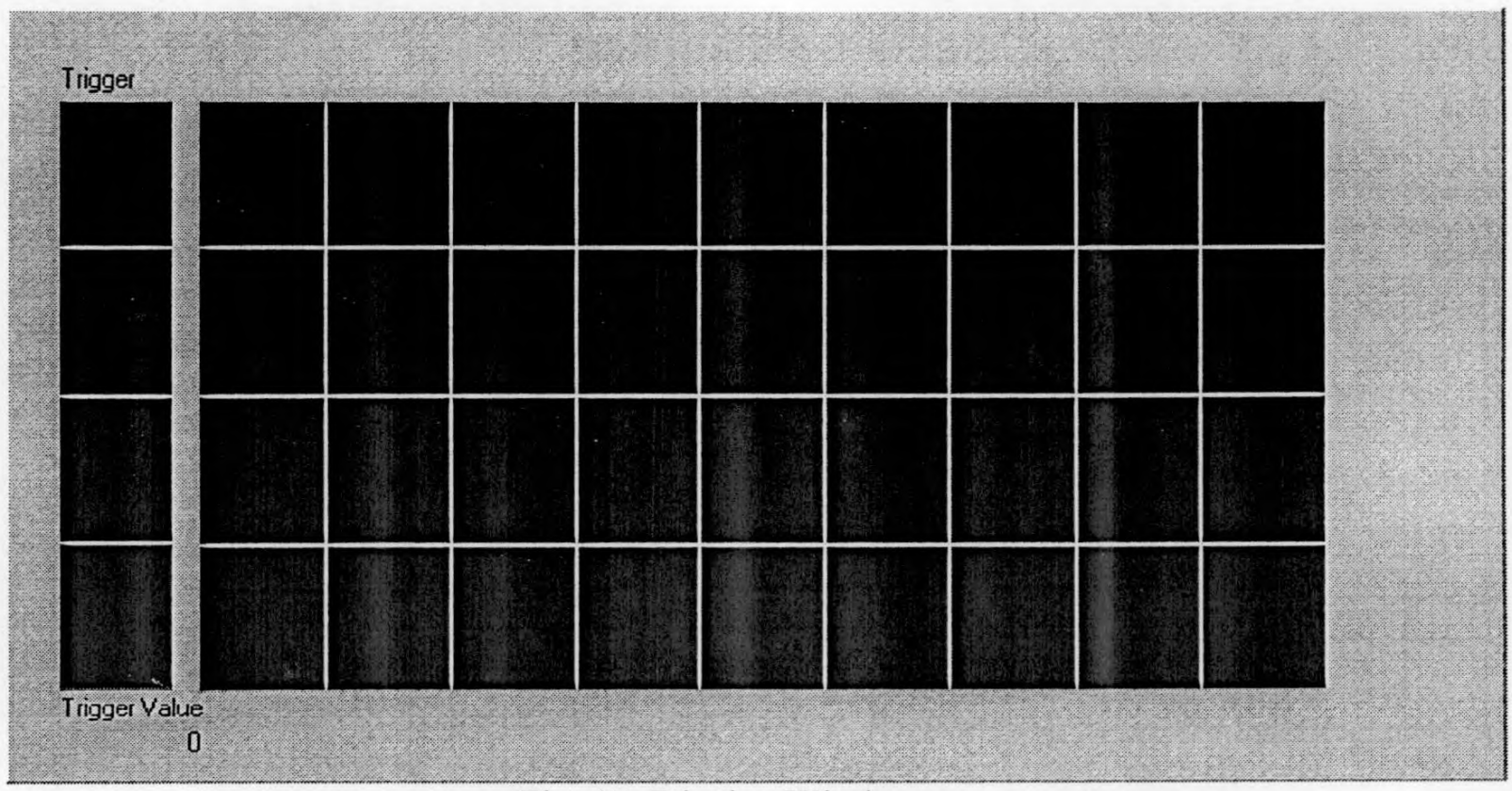


Fig. 17: Display Window

3.iv.j2.3 Circuit for Frequency Auto Scanning

The 1MHz IF signal can be converted to a base band signal by using a detector. This represents the instantaneous magnitude of the input signal which can be displayed in a CRO. In this way, the Y-axis displays the signal being detected while the X-axis displays the frequency, when the CRO is set to X-Y mode.

For this purpose, a scanning circuit was developed to vary the microwave VCO frequency and hence the input UHF frequency continuously and repetitively over the range of interest. The same scanning frequency is used to drive the X-axis of the CRO.

The following circuit in Fig. 18 generates a ramp signal with a peak to peak range of 7Vdc to 18Vdc which corresponds to a frequency range of 2700MHz to 3500MHz of the VCO. This translates to the selection of input signal frequency range of 400MHz to 1200MHz. The frequency of the ramp waveform is 70Hz.

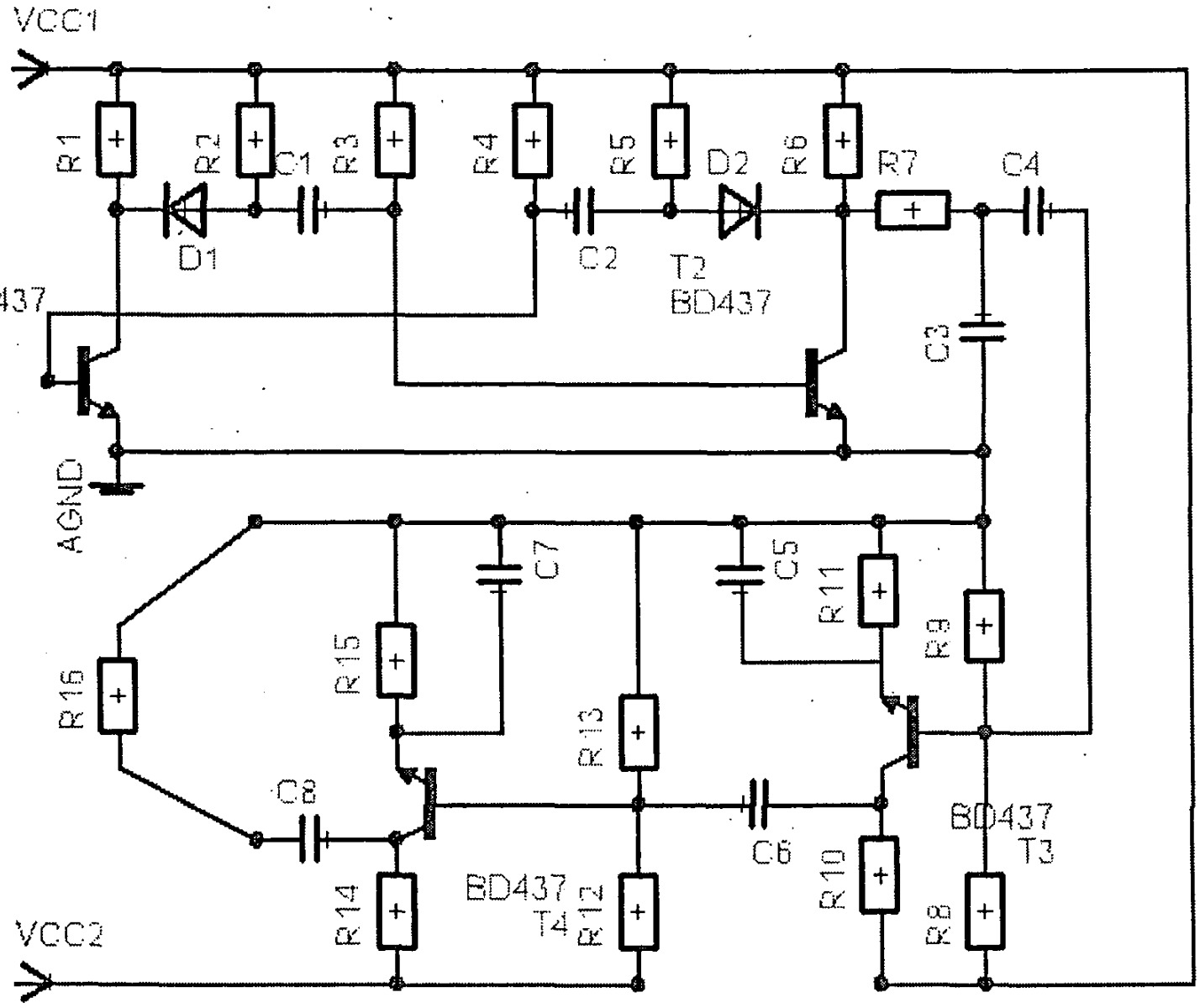


Fig. 18: Ramp Generator Circuit

The R7 and C3 integrate the rectangular waveform generated by the oscillator consisting of T1 and T2. This results in a ramp waveform with a peak magnitude of a few hundred millivolts. The preamplifier consisting of T3 increases the level of this signal to a few volts. Then, the large signal amplifier consisting of T4 raises this level to the required peak to peak range of 7 to 18 volts. The supply voltages VCC1 and VCC2 must be 5Vdc and 18Vdc respectively.

3.iv.j2.4 +18v, +12v and +5v regulated supplies

The ADJ of LM317K and LM317T has been set such that output voltages of 5, 12 and 18v are available at V_o. This is given by $V_o \approx 1.25(1+R_8/(R_2+R_5))$, for example for IC1. A supply voltage of 24 is connected to the V_{in}.

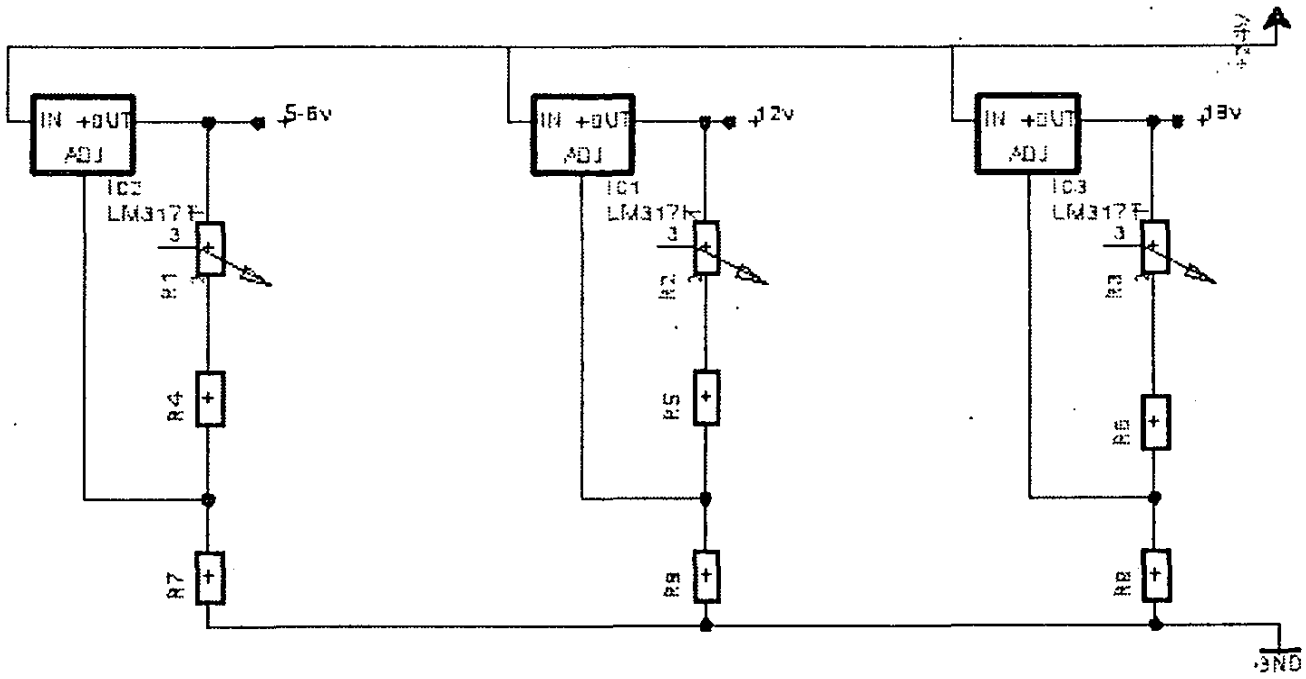


Fig. 19: Voltage Regulator Circuit

3.v.j Results and Outputs

Once the USB signal reader is provided with a 1MHz sinusoidal signal of 1v generated using a signal generator as in Fig. 20, the display window in Fig. 21 illustrates the magnitudes of current 512 signal samples. The energy meter and the power meter shows the energy accumulated over a 4ms interval (20480 samples) and the average power readings as 0.0019 Joules and 0.51 Watts.

Fig. 20: USB Digital Signal Reader Setup

They should be 0.0020 Joules and 0.50 Watts but different sets of readings proved that the accuracy remains at this level. The discrepancy is caused by the fact that the input voltage could not be set to 1.0v exactly.

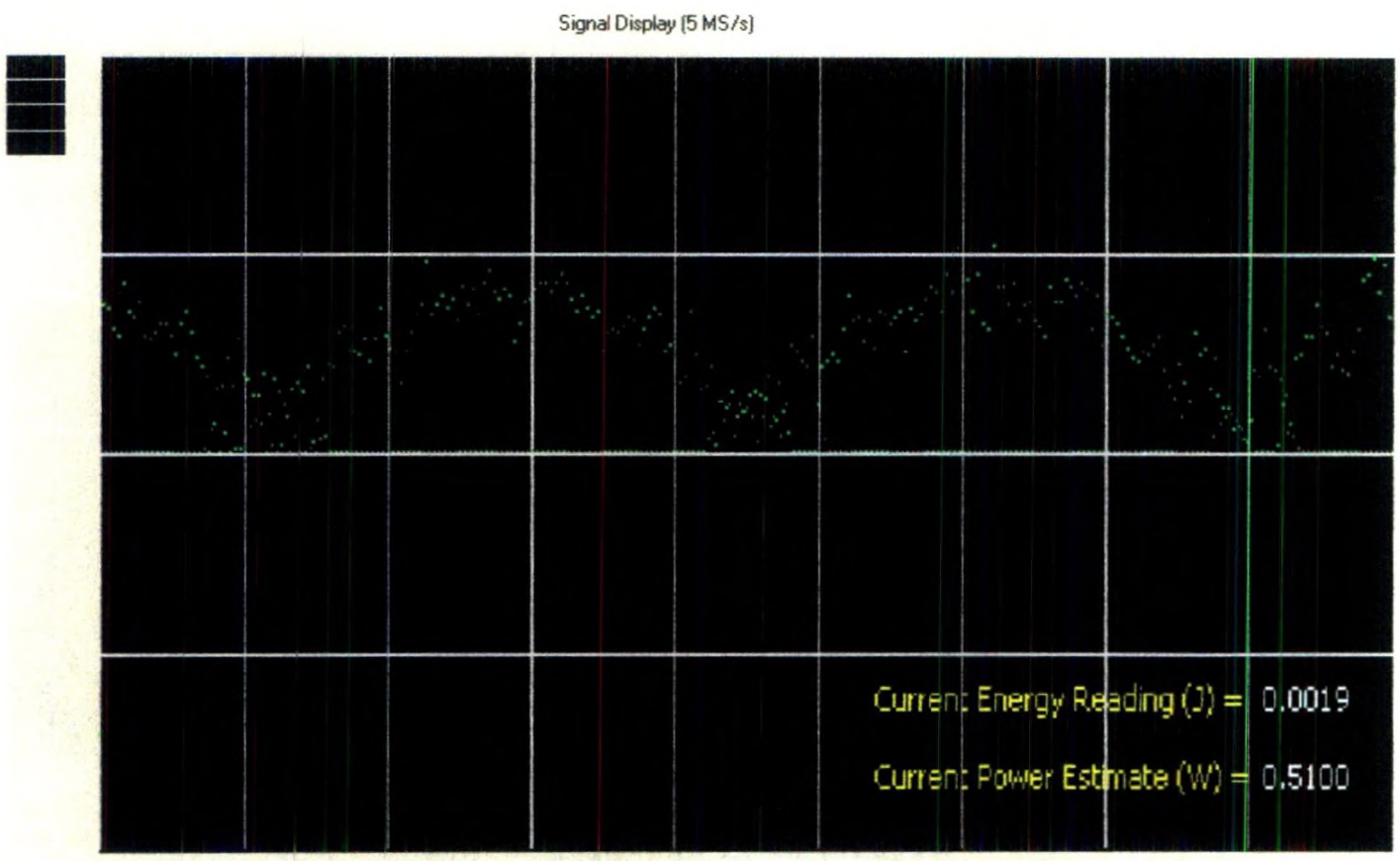


Fig. 21: Active Display Window Illustrating a 1v Sinusoidal Signal

Therefore, the comparison of measured energy and power and the real quantities in Table 1 were obtained by increasing the measurement period to 10ms. The small discrepancy for small voltages is again due to the difficulty of setting the input voltage exactly.

Peak Voltage (v)	Real Power (W)	Measured Power(W)	Real Energy (J)	Measured Energy (J)
0.1	0.005	0.0052	0.00005	0.0001
0.2	0.02	0.017	0.0002	0.0002
0.5	0.125	0.12	0.00125	0.0012
1.0	0.5	0.5	0.005	0.005
1.5	1.125	1.1	0.0125	0.011
2.0	2.0	2.0	0.02	0.02

Table 1: Energy and Power Measured over a Time Period of 10ms

Readings were repeated at random times in order to establish the variance of the error. The test signal used for this purpose had a peak voltage of 1v where the signal power was 0.5W. Table 2 shows that the measurement error is less than 10mW.

Measured Power(W)	0.50	0.49	0.50	0.50	0.50	0.50	0.51	0.50	0.50	0.50
|Error| (W)	0.00	0.01	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.00

Table 2: Measurement Error for 1v, 0.5W Signal

The frequency auto scanner circuit was connected to the VCO of the microwave up-convertor as illustrated in Fig. 22. Although this selects a range of input frequencies from 400MHz to 1200MHz as the VCO frequency is varied up and down, demonstration is not possible because signals are not available over the whole range. Therefore, instead, the variation of the up-converted frequency is displayed in the spectrum analyzer by keeping the input RF frequency fixed at 800MHz. The display of the spectrum analyzer in Fig. 23 shows the resulting frequency variation from 1900MHz to 2700MHz. Note that the scanning frequency is 70Hz and therefore the spectrum analyzer can display only a few spectral lines at this rate.

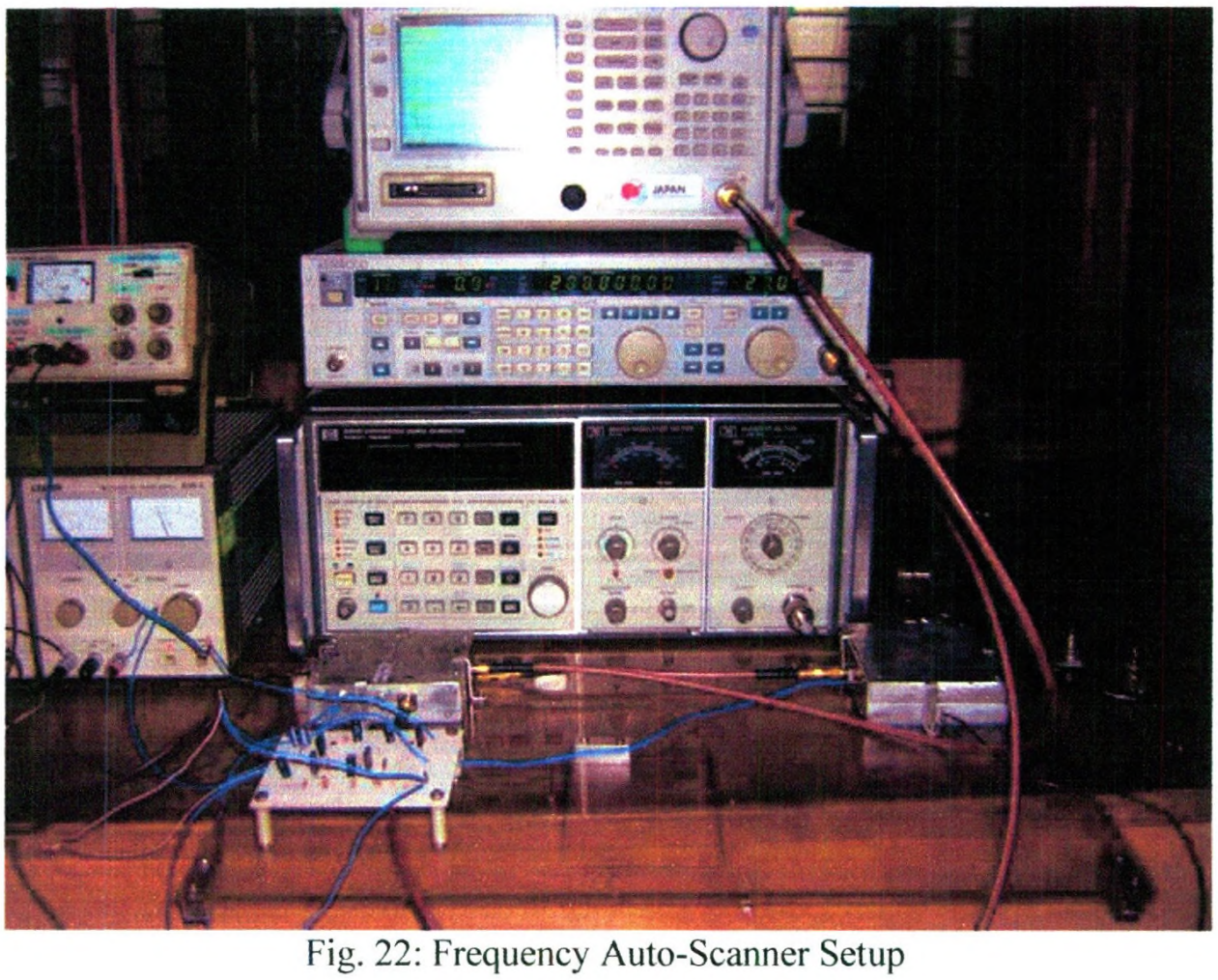


Fig. 22: Frequency Auto-Scanner Setup

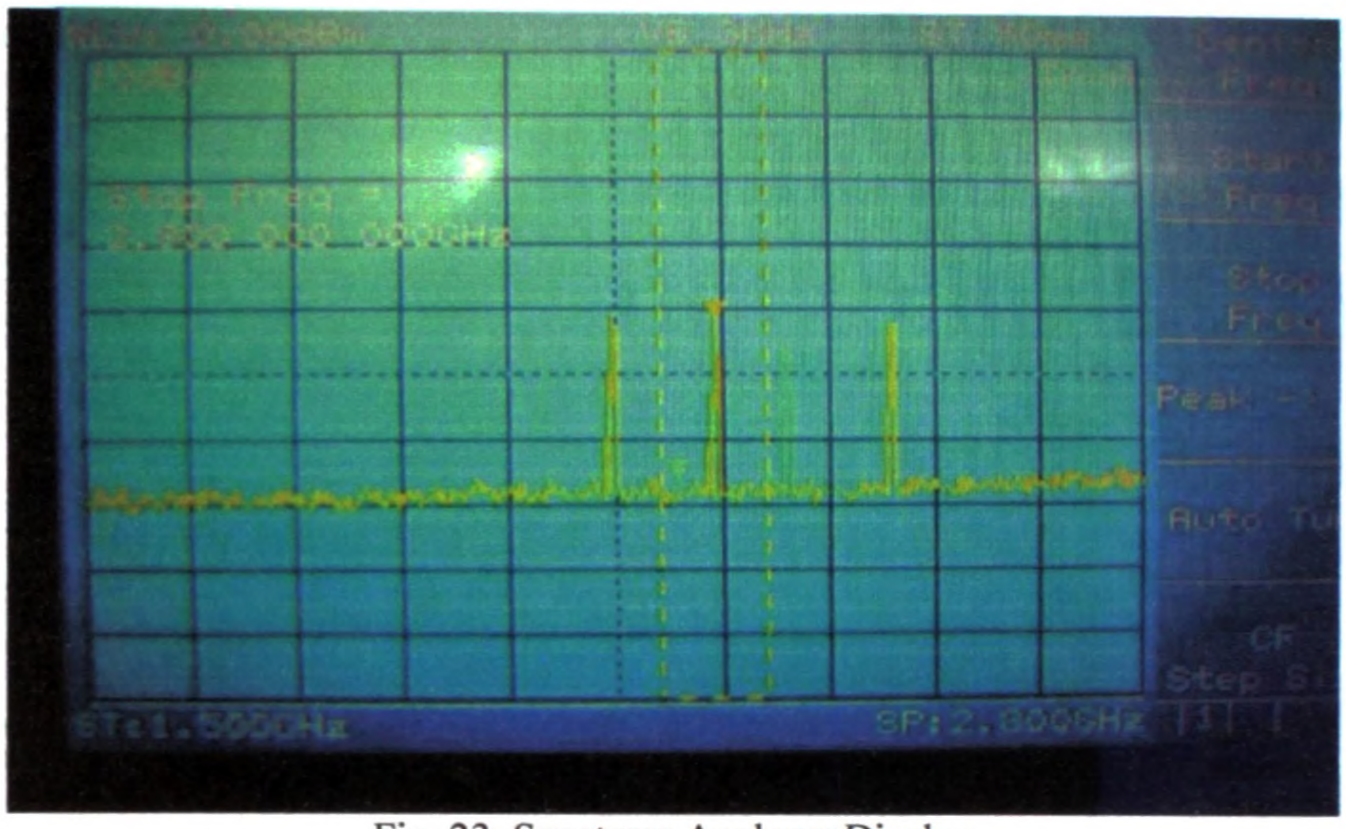


Fig. 23: Spectrum Analyser Display

3.vi.j Discussion

Because the 1MHz signal is sampled into the Delphi program at a rate of 5MS/s, the energy and power measurements should be exactly correct. The very small discrepancy between the exact values and the measured readings presented in the results section is due to the instability of the input signal generated by the very old signal generator. The accuracy of the measurement would be much better if the signal generator produced a more stable signal.

3.vii.j Problems Encountered

Throughout the project period, there were difficulties in obtaining components, whenever needed. The Maxim 1426 integrated circuit was received as a free sample from the manufacturer. It was not possible to find a supplier who would sell a few items of this type. The minimum order quantity was found to be 100's or more, which would be unaffordable and wasteful.

Later, when improvements to the circuits were planned, it was found that the manufacturer would not even send free samples any longer.

3.viii.j References

[1] Frederic, P. (2007), "ITU Document MMSM/03", Geneva, 22-23 January.

[2] MicroChip PIC18F4550 (2004), http://www.microchip.com/.

[3] MAXIM 1426 (2000), http://www.maxim-ic.com/.

[4] Ciarcia, S.A. (2002), "ADPCM for highly intelligible speech synthesis", http://werdav.tripod.com/adpcm.html.

[5] Feldman, A R. et al. (1998), "A 13-bit, 1.4MS/s Sigma-Delta modulator for RF based applications", IEEE Journal of Solid State Circuits, 33(10): 1462-1469.

3.ix Overall Performance of the Signal Meter

3.ix.1 Calibration of Microwave and RF Circuits Using a Spectrum Analyser
(Signal Source: Kenwood SG7130, Spectrum Analyser: Anritsu MS2661C)

There are two microwave circuit modules and one RF circuit module fabricated for the signal meter. The microwave modules contain gain amplifiers for increasing the signal level and compensate for mixer and filter losses. The RF module contains two passive elements, the SAW filter and the mixer, which cause a loss of 16dB. The main target of this calibration is to establish the overall gain or loss over the input UHF frequency range and for the expected dynamic range of the input signals.

The UHF to 2.3GHz up-covertor module is connected to the micro-strip filter which provides a 2.3GHz signal with a bandwidth of 100MHz. This signal frequency is down converted to 63MHz using the next microwave circuit module. Both microwave circuit modules are powered by a 12vdc supply and, in addition, the tuning voltage in the up-convertor module for selection of UHF frequencies is supplied by another 3-18vdc source. The 63MHz signal is filtered to a 3dB bandwidth of 400kHz by the SAW filter in the 63MHz to 1MHz down-convertor module. The power of the 1MHz IF signal is measured using the spectrum analyzer. Fig. 1 and 2 illustrate the experimental setup used for the calibration.

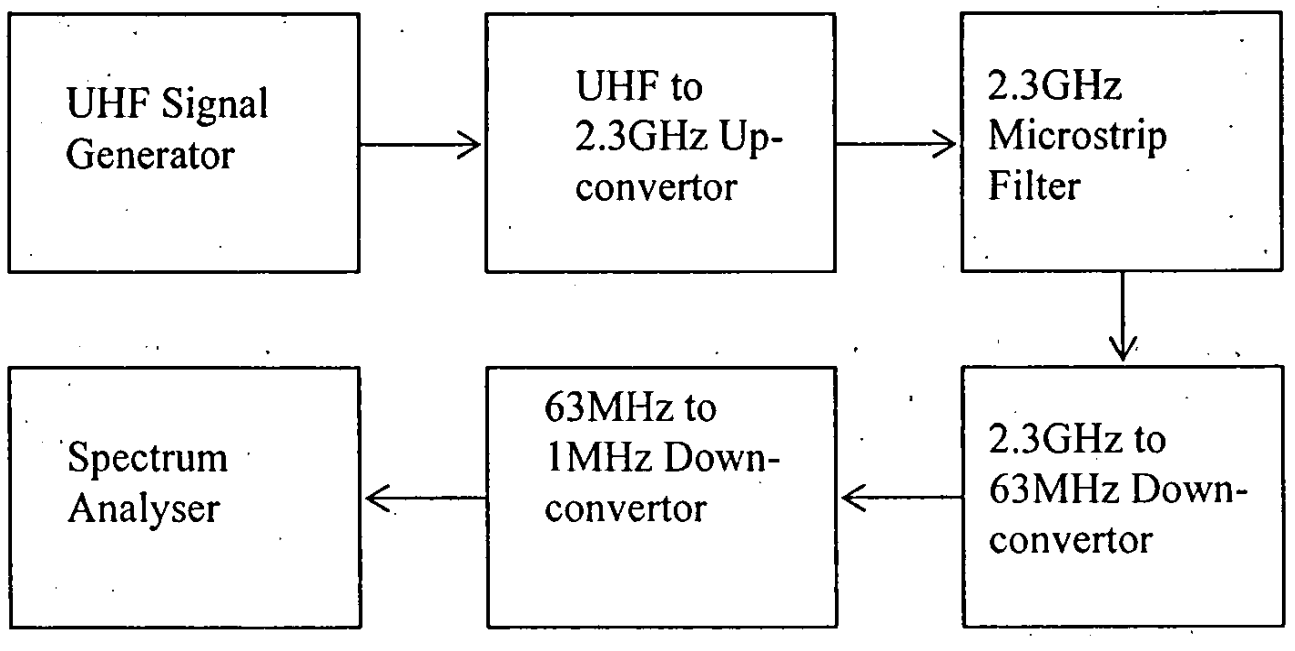


Fig. 1: Calibration Setup 1

Fig. 3 illustrates the overall loss of the microwave and RF modules for the input dynamic range of -30 to -70dBm at a constant frequency of 800MHz. For example, if the measured power of the unknown signal at 800MHz happens to be -70 dBm, the real power is 7dBm higher. Fig. 4 illustrates the same for the UHF frequency range of interest while keeping the input signal level fixed at -50dBm. Therefore, a calibration curve must be used for each input frequency for precise measurements. However, if 1 or 2 dBm can be tolerated, one calibration factor (gain or loss), rather than a curve over the whole dynamic range, can be used for a given frequency.

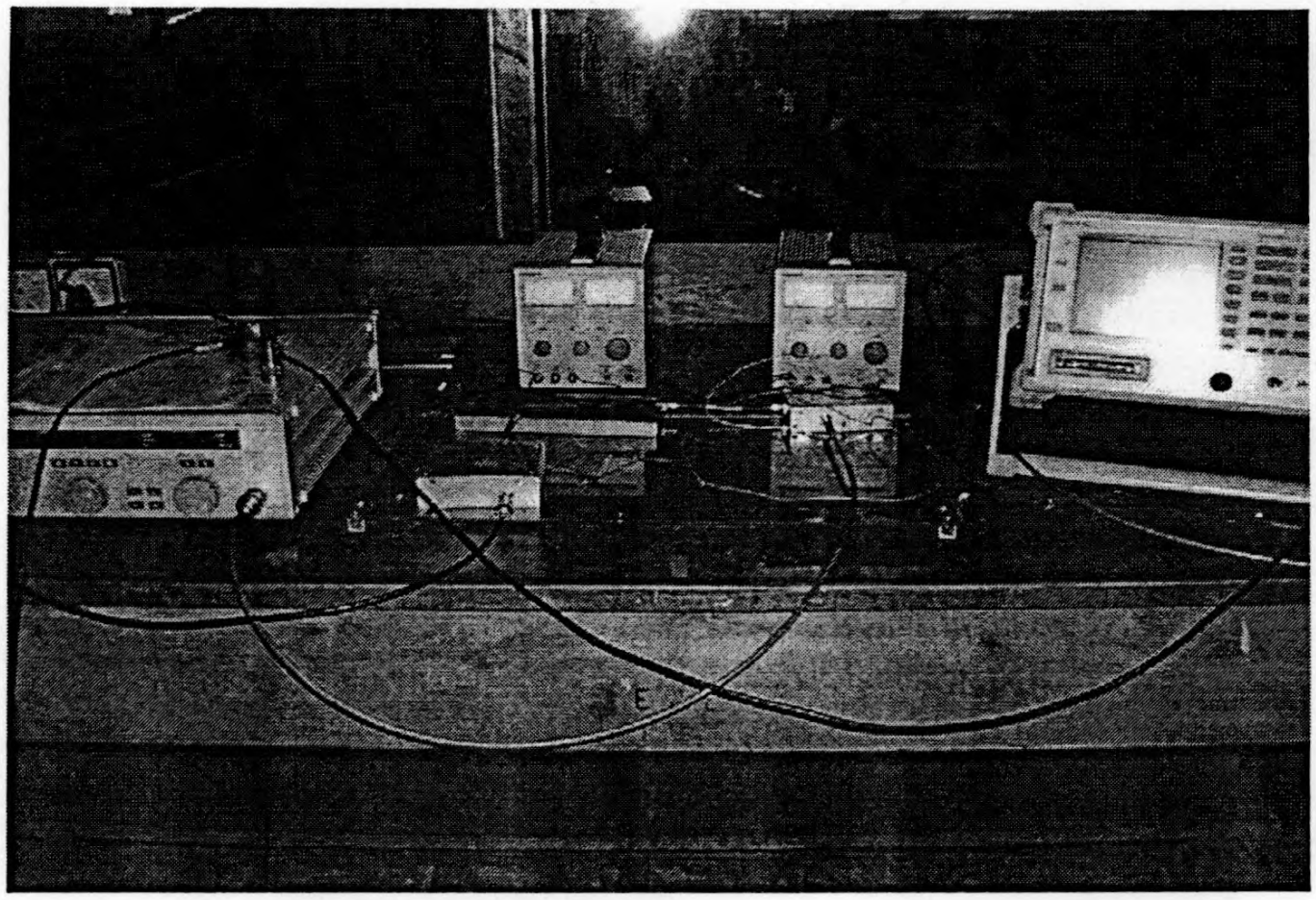


Fig. 2 Photograph of the Calibration Setup 1

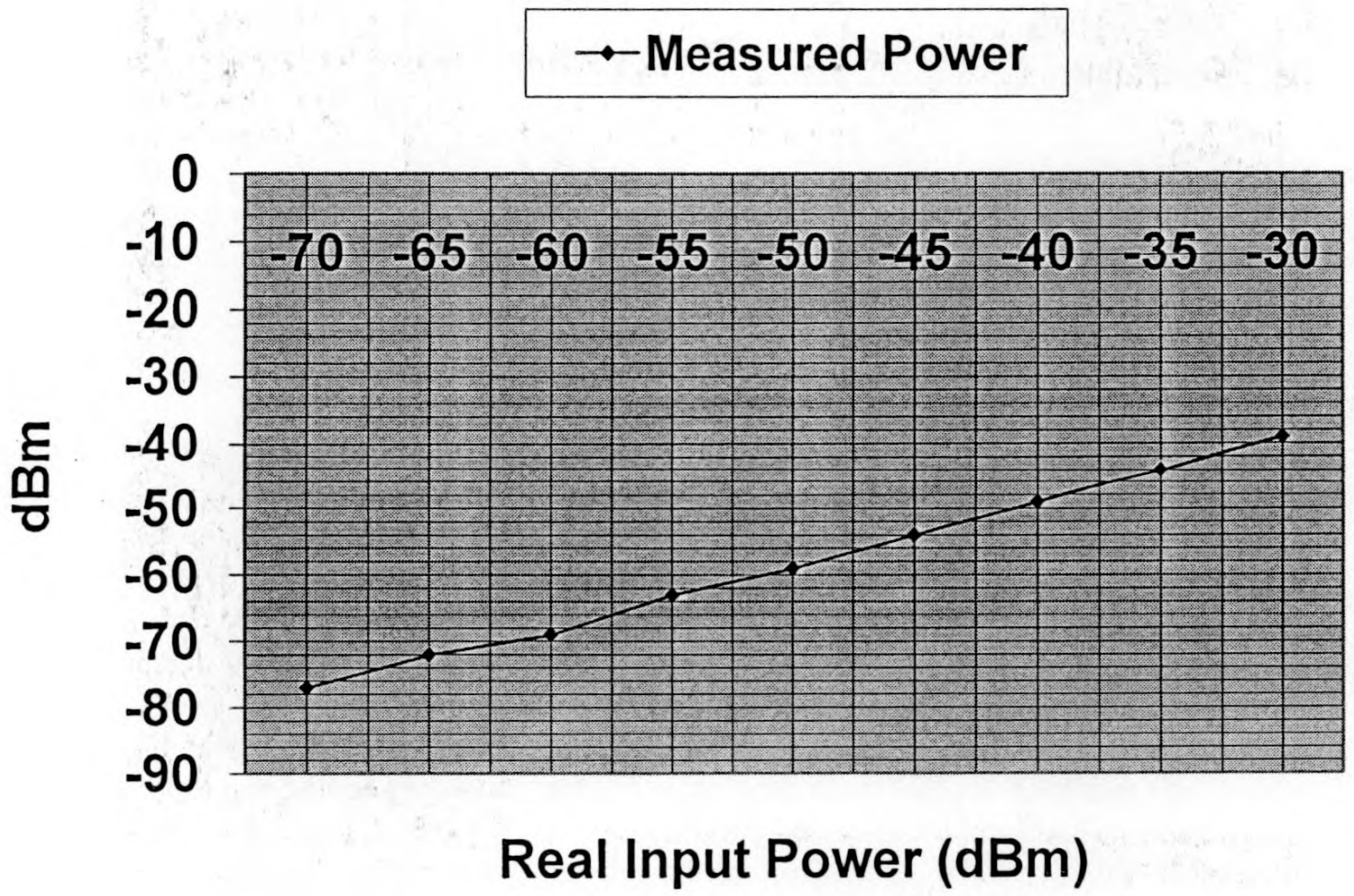


Fig. 3: Measured Power at 800MHz

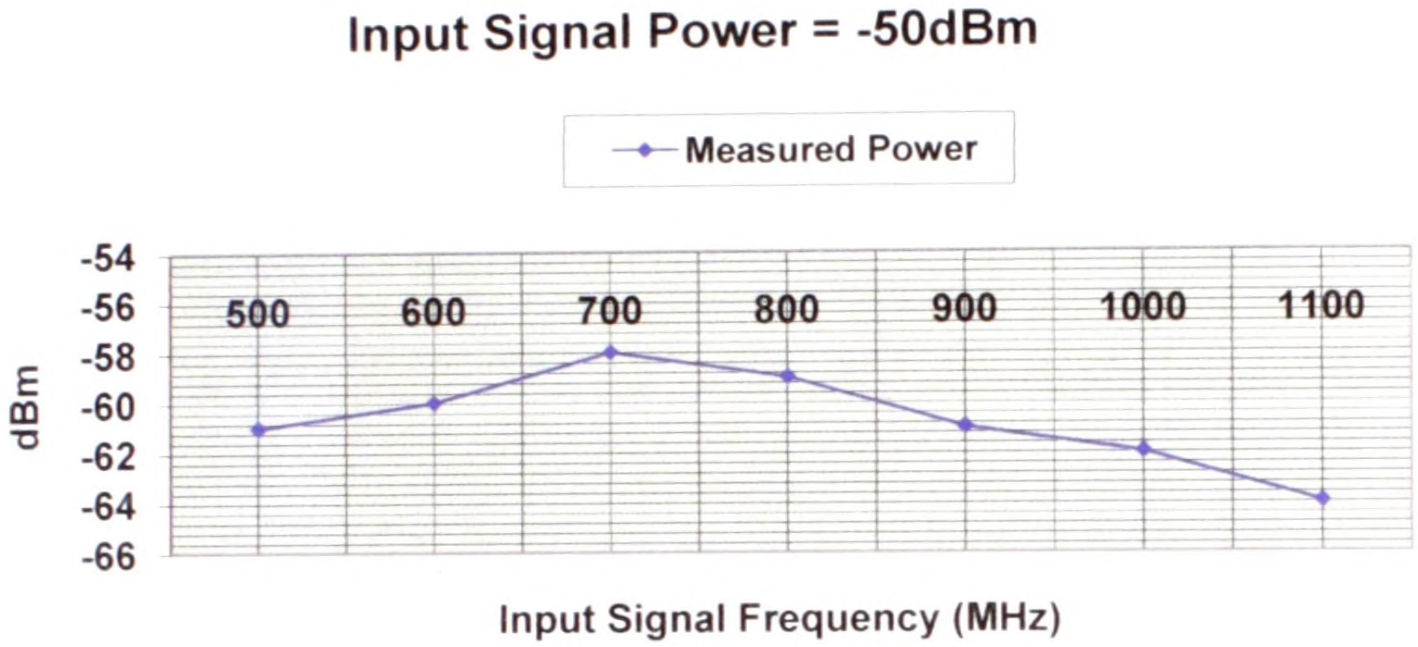


Fig. 4: Calibration Curve for Input Frequency Variation

3.ix.2 Calibration of Microwave and RF Circuits Using an Oscilloscope
(Oscilloscope: LEADER LBO 523)

Instead of the spectrum analyzer shown in Fig. 1, the 1MHz IF signal was displayed in the oscilloscope. Fig. 5 illustrates the down-converted 1MHz sinusoidal signal waveform in the oscilloscope screen while Fig. 6 illustrates the signal voltage for the input dynamic range from -30 to -60dBm. The input signal frequency was fixed at 800MHz.

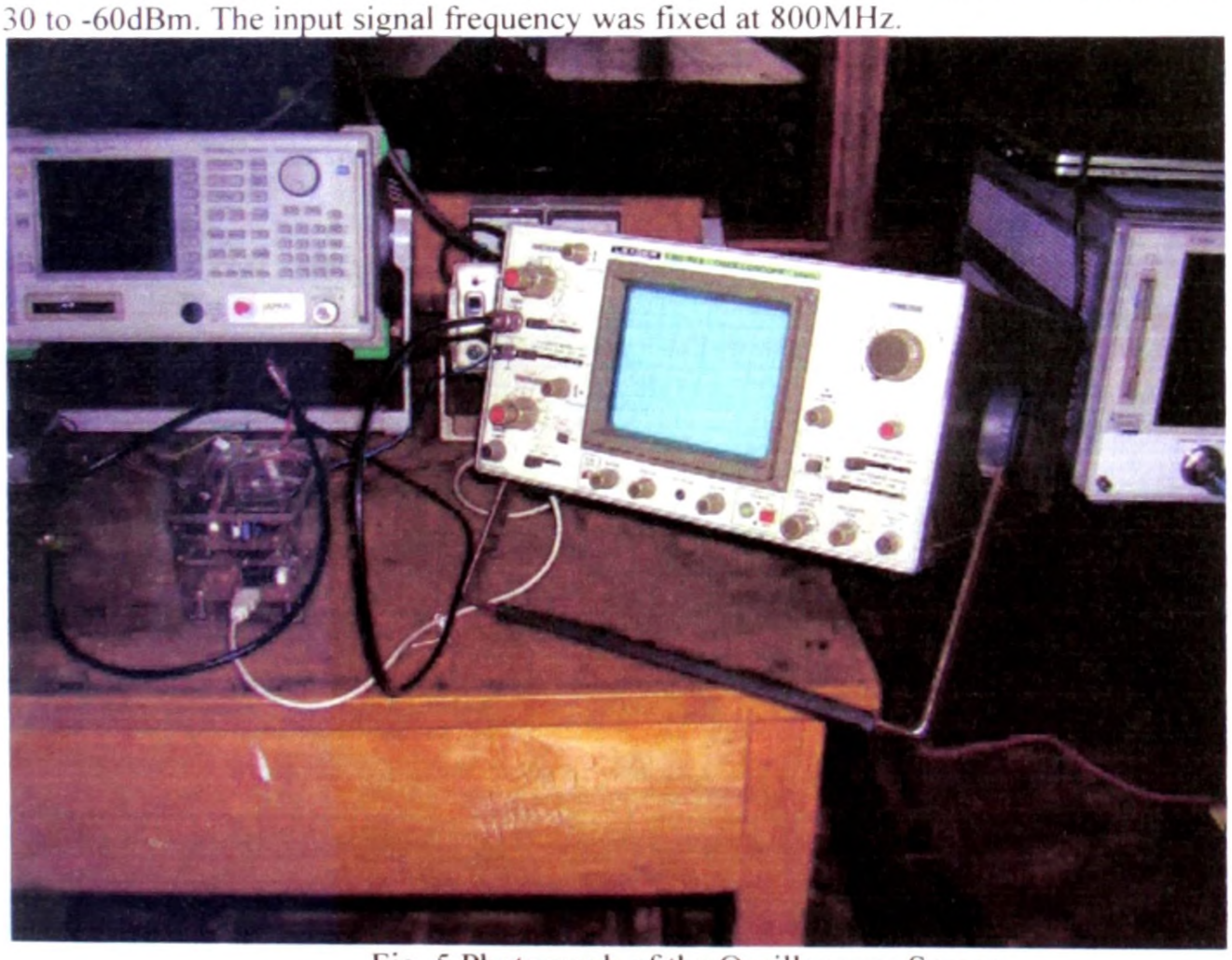


Fig. 5 Photograph of the Oscilloscope Screen

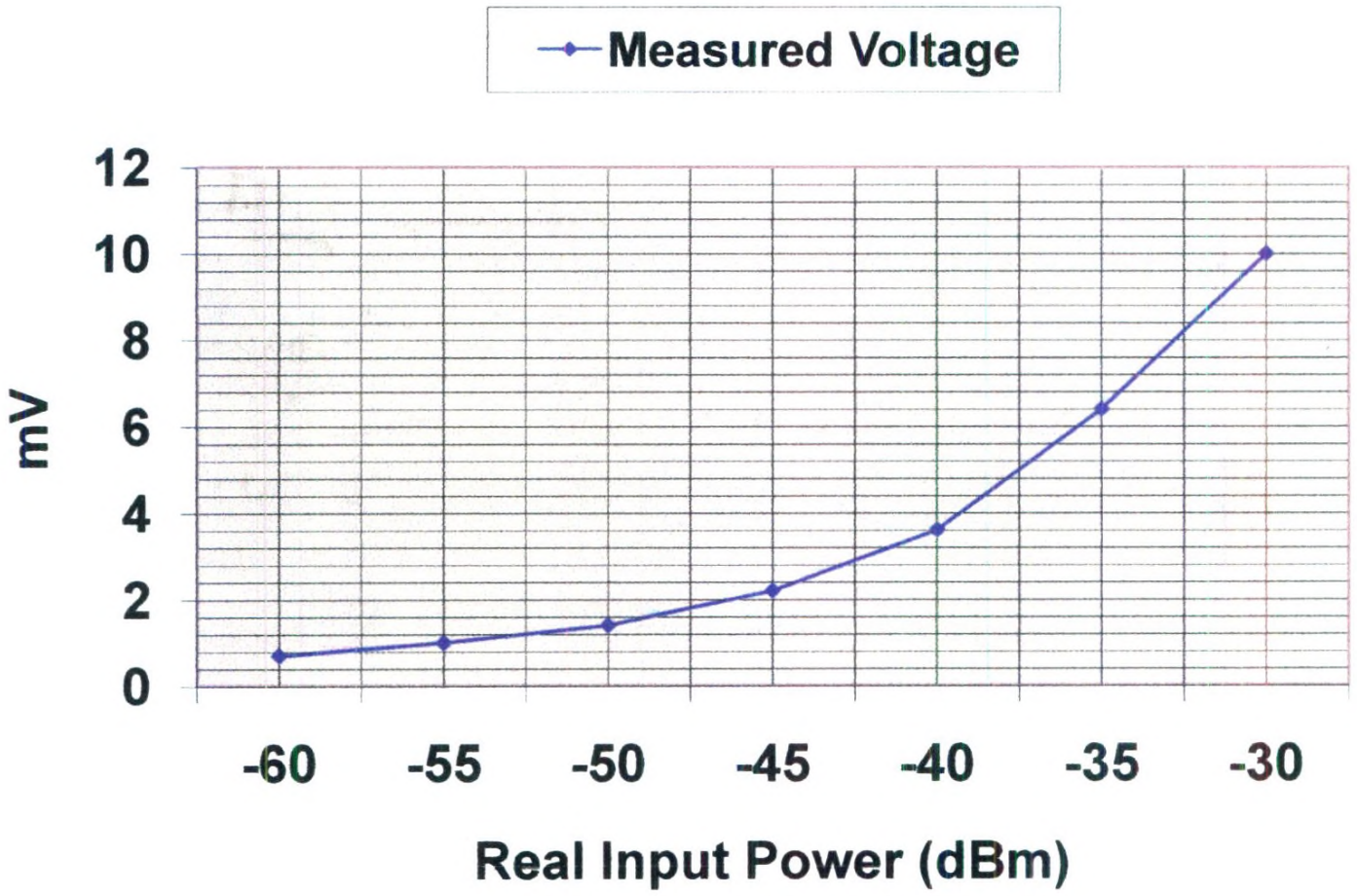


Fig. 6: Measured Peak-to-Peak Voltage at 800MHz

3.ix.3 Calibration of the overall system Using the USB Signal Reader

The 1MHz IF signal was read using the USB reader as described in sections 3.iv.j2 and 3.v.j. The laptop computer displays the instantaneous signal voltages, the energy reading and the power reading. Since the maximum peak-to-peak voltage of the 1MHz signal happens to be less than 10mV (for -30dBm input), further amplification is provided using the 1MHz amplifier before reading into the computer. This is because the input resolution of the A/D convertor inside the USB reader is 20mV, peak-to-peak. Note that the software of the computer display associated with the USB reader has to be modified for a given amplifier.

Fig. 7 and 8 illustrate the system setup with a close up of the display.

Fig. 7: Photograph of the Signal Meter with External Signal Generators and Power Supplies

Fig. 8: Computer Display with Energy and Power Readings

Section 4

Impact of Research Results

4.i Relevance of results achieved to scientific advancement

Mobile and wireless devices which use the UHF radio spectrum is very common. Most of these equipment transmit and receive UHF signals within their allocated cells. The complete signal meter will help measure the signal strengths within a cell allowing to establish cell boundaries. The base station which connects all the users in the cell to those in other cells is equipped with an antenna with a radiation pattern similar to the cell shape. Therefore, the signal meter can be used in the design and testing of antennas with the required radiation pattern.

The experience gained during the project period will be useful in the future to construct better microwave circuits. These customer made circuits help carry out various scientific experiments.

4.ii Relevance of results achieved to national/socio-economic development

New equipment, accessories and component kits for microwave PCB fabrication were obtained through this grant. This enhanced the capacity of the microwave research facility in the department of electrical and electronic engineering, University of Peradeniya to construct microwave circuits. A considerable number of microwave products, such as mobile equipment, Bluetooth, IEEE 802.11, TV and radio transmitters/receivers, are available in the market today. Their prices vary from cheap to expensive. With the experience acquired throughout the project period, it will be possible in the future to manufacture at least some of such products locally. These will provide a cheaper option for prospective users.

4.iii Methods adopted and/or proposed for the dissemination/application of research outputs

Three publications have been made so far in conference proceedings. It is planned to make a full publication covering the activities and outcomes of the whole project in an appropriate conference or a magazine.

It is hoped that the final report and the previous progress reports provided to NSF will disseminate the knowledge and experience gained through this programme to collaborating persons and organizations.

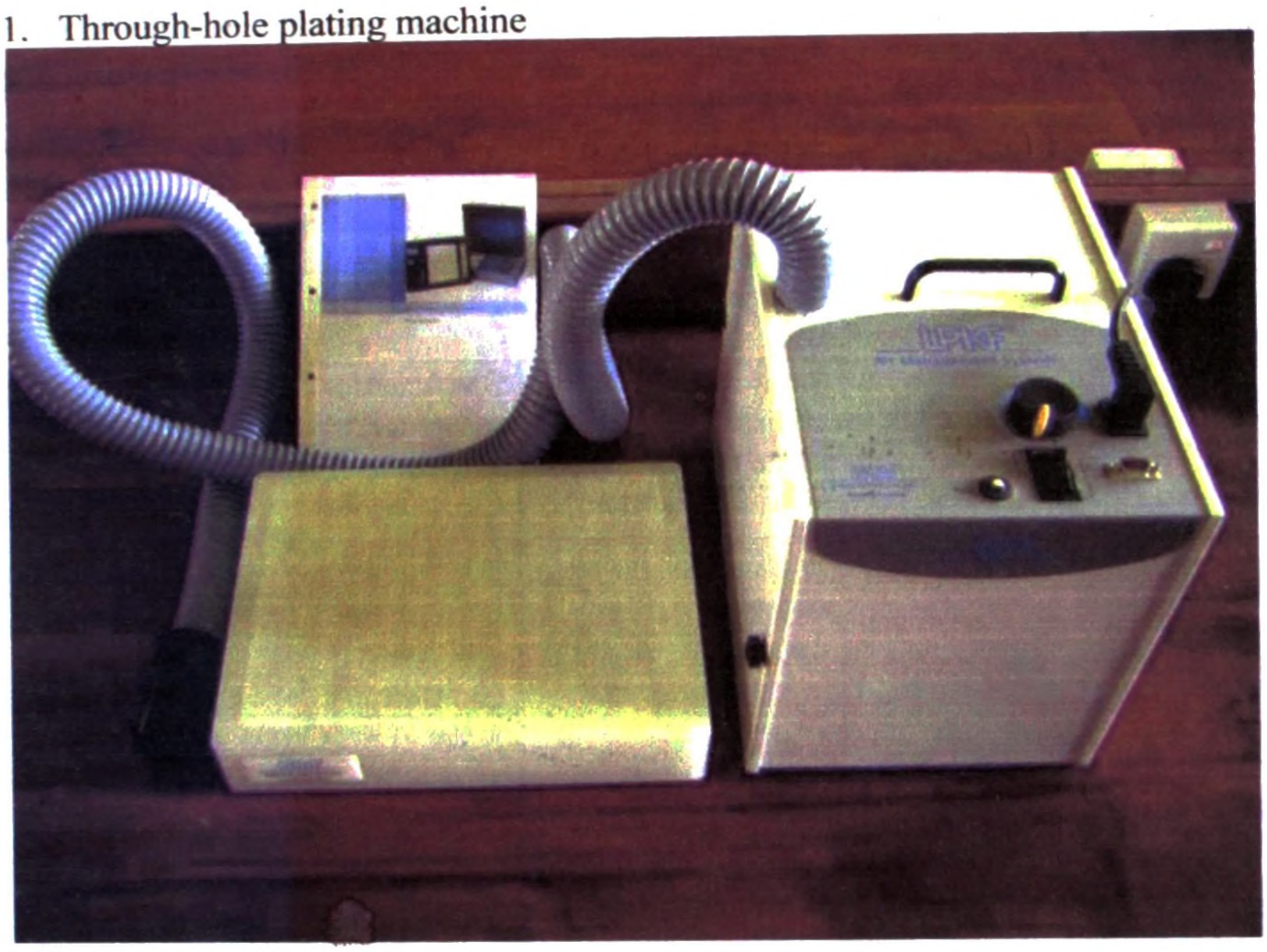
It is planned to approach Institution of Engineers, Sri Lanka to arrange a seminar.

Section 5:

Miscellaneous

5.i List of major equipment acquired during the project period and their functionality

1. Through-hole plating machine



2. Microwave integrated circuits (Amplifiers, VCOs, Mixers), high grade, surface mount resistor, inductor and capacitor kits, antenna components

Item	Type	Description	Units
1. K1-ERASM+	Amplifier Amplifier Amplifier Test Board	ERA-1SM+ ERA-2SM+ ERA-3SM+ TB-40B-1+	10 10 10
2. SIM-U742MH+	DBL BAL Mixer		10
3. ROS-3360+	VCO		5
4. TCCH-80+	RF Choke		10
5. MBA-15LH	DBL BAL Mixer		10

6. ROS-2252+	VCO		5
7. HELA-10D	BB Amplifier		1
8. KIT14-B-2512-F	Resistor Kit		1
9. KIT12-B-2512-F	Resistor Kit		1
10. Design Kit 14T	Capacitor Kit	1000 - 5100 pF	1
11. Design Kit 25T	Capacitor Kit	0.1 - 2.0 pF	1
12. Design Kit 26T	Capacitor Kit	1.0 – 10 pF	1
13. Design Kit 27T	Capacitor Kit	10 – 100 pF	1
14. Design Kit 35T	Capacitor Kit	100 – 240 pF	1
15. L060 10-20	Inductor Kit		1
16. C08-50	Capacitor Kit		1
17. PE3656LF-12	Semi rigid bare-copper coaxial cable (PE-047SR) with connectors	SMA male- SMA male, length 12", Diameter 0.047" (1.2 mm), 50 Ω	2
18. PE34191LF-12	Semi rigid bare-copper coaxial cable (PE-020SR) with connectors	SMA male- SMA male, length 12", Diameter 0.020" (0.508mm), 50 Ω	2
19. UT085	Cable	Semi-rigid Coaxial	6
20. SM3310	Adapter	3.5mm/M, 34GHz	1
21. SM3315	Adapter	3.5mm/F, 34GHz	1
22. SM3310	Adapter	3.5mm/F, 34GHz	1

3. Gold plating chemicals and accessories
4. Tin plating chemicals and accessories

5.ii List of publications

1. Jagath-Kumara K D R (2009), "Design and Fabrication of an RF Energy Meter – Part 1: Signal Acquisition and Energy Estimation", *Proceedings of Peradeniya University Research Sessions*, p 513-515, Vol 14, Part II, 3 Dec.

2. A U A W Gunawardena (2009), "Design and Fabrication of an RF Energy Meter – Part 2: The design of the RF front end", *Proceedings of Peradeniya University Research Sessions*, p 516-518, Vol 14, Part II, 3 Dec.

3. Disala Uduwewala (2009), "Design and Fabrication of an RF Energy Meter – Part 3: Antenna for power density measurements", *Proceedings of Peradeniya University Research Sessions*, p 519-521, Vol 14, Part II, 3 Dec.

Section 6

Summary Statement of Expenditure (indicate under Personnel, Equipment, Consumables, Travel and Subsistence and Miscellaneous)

Our Ref :- AB/Eng/13-07-177-00-207

The Financial position of grant no.RG/2007/SI/02 as at 03.08.2010 awarded to Dr. K.D.R. Jagath Kumara...by National Science Foundation is as follows.

		Funds received/ By the Univ/ Institution	Total expenditure Rs.	Balance available Rs.
Man Power		100,000.00	103,026.49	(3,026.49)
Personnel	-Research Student	-	-	-
	Technical Assistant	-	-	-
	Other	-	-	-
Equipment	- Foreign	300, 000.00	300,000.00	-
	- Local	-	-	-
Consumables	-Foreign	400,000.00	416,029.47	(16,029.47)
	Local	120,000.00	120,000.00	-
Travel & Subsistence		-	-	-
Miscellaneous		30,000.00	30,000.00	-
Total		**950,000.00**	**969,055.96**	**(19,055.96)**

Unspent balance of Funds received	Rs.
Funds received	950,000.00
Actual expenditure	(969,055.96)
Balance	(19,055.96)
Cash Impest/ Cash Advance	-
Outstanding Commitments	-
Balance as at 03.08.2010	**(19,055.96)**

Assistant Bursar
Faculty of Engineering

03 · 08 · 2010
Date

Asst. Bursar
Faculty of Engineering
University of Peradeniya

Section 7

i) Grantees' signatures

1.
2. A.W.A.W.
3.

ii) Comments of the Head of the Department/signature

successfully completed. Three research papers were presented at the undergrad research session. Excellent progress was observed. The experimental setup and associated modules are innovated for the first time in Sri Lanka (accordings to the discussion with the staff members).

A. A.
27/10/2015.

iii) Head of the Institution's signature

RECOMMENDED & FORWARDED

DEAN
FACULTY OF ENGINEERING,
UNIVERSITY OF PERADENIYA,
PERADENIYA, SRI LANKA.

27/10

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